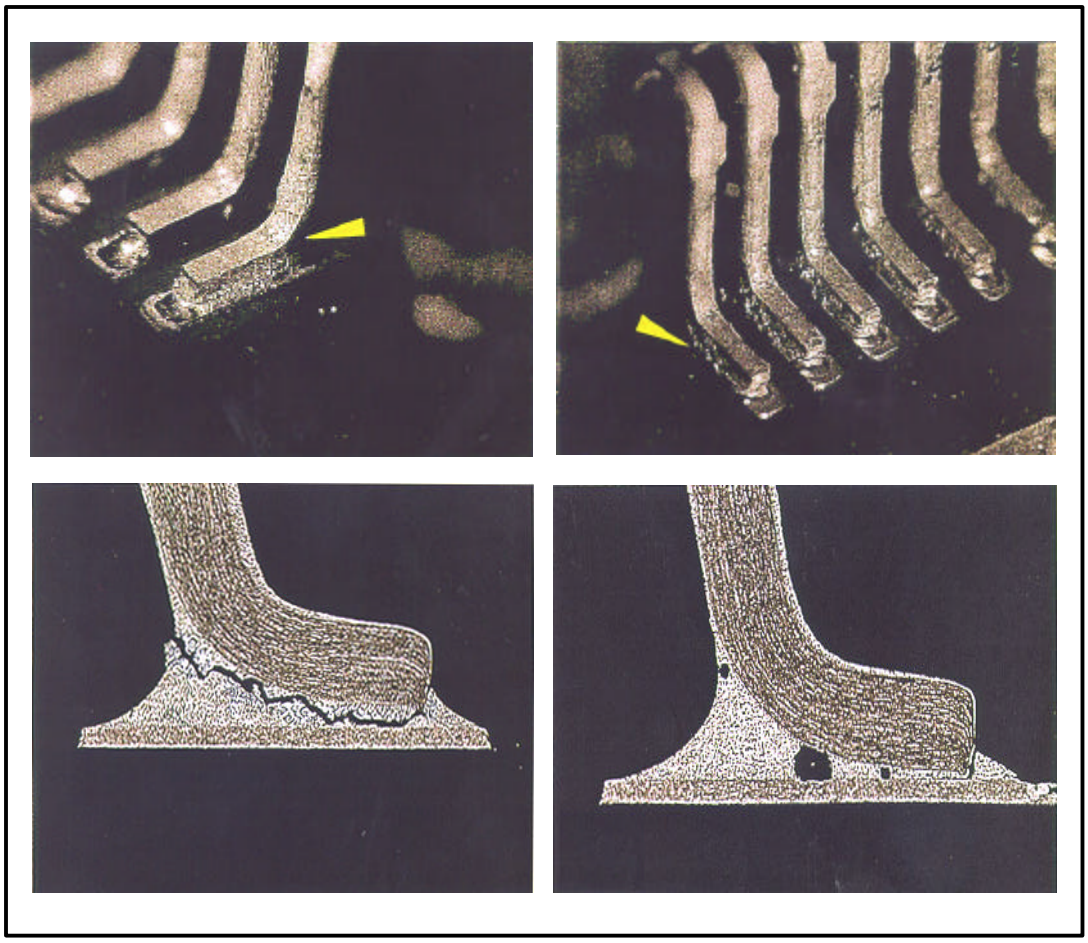
ELECTRONIC PACKAGING & SPACE PARTS NEWS

EEE Links

January 1998, Vol. 4 No. 1

In this issue:



Editor: **Robert Humphrey, (301) 731-8625**
rhumphre@pop300.gsfc.nasa.gov
Mailing List Information and Article Submissions: (301) 731-8625
Desk Top Publisher: **Esther Bailey**
Published by the NASA/GSFC Electrical Systems Center
Components Technology and Radiation Effects Branch, Code 562
Branch Head: **Robert Lebair**

WWW URL Address:
http://arioch.gsfc.nasa.gov/312/Linkspg.html

The cover photograph shows cracked gull-wing solder joints (left top and bottom) resulting from Mechanical Deflection System (MDS) testing, and similar cracking resulting from Thermal-cycling. (Right top and bottom). *(See Article on page 2).*

c o n t e n t s

Articles

Articles

Letter from the Editor

Robert Humphrey
Editor of EEE Links
(301) 731-8625
rhumphre@pop300.gsfc.nasa.gov

Welcome to the January issue of EEE Links. This issue, as in past issues, contains a wide variety of articles on technological and procedural advances. Keeping abreast of the latest technology continues to be a challenge in our continually changing and dynamic environment. Sharing information is vital in meeting NASA's goal of smaller, better, cheaper and faster space flight missions.

As always, please keep us informed of your questions and needs so that we may be able to serve you better.

NASA/SEMATECH/SRC SYMPOSIUM

Michele M. Gates
Technical Validation Assurance
Assurance Technology Division
NASA Goddard Space Flight Center
(301) 286-1260
Michele.M.Gates.1@gsfc.nasa.gov

The *NASA/SEMATECH/SRC 1st Symposium on Soft Errors, Radiation Effects, and Reliability in VLSI: Terrestrial Applications* was held October 27 and 28, 1997 at NASA Goddard Space Flight Center in Greenbelt, MD. The meeting was extremely successful, drawing approximately 100 attendees from many U.S. and Japanese commercial semiconductor manufacturers, government agencies and laboratories, universities, and a mix of IC users representing the computer, health care device, aeronautics, defense, and space industries. International participation included individuals from Japan, France, Belgium, Uzbekistan, Ukraine, Surrey, Sweden, United Kingdom, Russia, and Germany. Soft errors were discussed as a reliability issue for current memory technology, as impacts to logic are an emerging concern.

Presentations were grouped into four technical sessions: Embedded Applications, Sub-micron Technology Issues, Soft Errors and Reliability, and Test Facilities. Invited presentations included: "Single Event Effects on the Ground – Neutrons as the Main Cause," by Eugene Normand of Boeing Defense & Space; "Deep Sub-micron Process Architecture Challenges and Their Impact on Soft Errors and Radiation Hardness," by P.K. Vasudev of SEMATECH; "Challenges in Modeling Soft Errors in Complex Sequential Logic," by Lloyd Massengill of Vanderbilt University; "Nuclear Processes Relevant for Single Event Upsets," by Henry Tang of IBM MSR&D Laboratory; and "Solutions for Space: Lessons Learned," by Ken LaBel of NASA Goddard Space Flight Center. The open forum, which included a panel discussion with members from Intel, IBM, AMD, Boeing, and Sandia National Lab, spurred some very interesting technical exchange among the conference attendees. Plans are in progress for a second conference to be held during the same time frame in 1998.

ASAP Activity at Goddard

Qutub GhulamAli
NASA Parts and Packaging Program
Goddard Space Flight Center
Greenbelt, MD 20771
(301) 731-8689
qghulama@pop300.gsfc.nasa.gov

The NASA Active Supplier Assessment Program (ASAP) activity at Goddard is working on updating the NASA Core Suppliers List (CSL) Part I and the Vendor Information Matrix (VIM) along with a new section, the Advanced Technology Devices Listing, for release early this year via the NASA web site at http://arioch.gsfc.nasa.gov/311/html/311.html.

The revised CSL Part I will reflect changes required for greater consistency between the part types and manufacturers that are listed in this document and those that are listed in the VIM.

New devices such as ACS/ACTS from UTMC which are Bulk CMOS rad hard/SEU tolerant and the Silicon-on-Sapphire (SOS) technology from Harris which are also rad hard/SEL Immune/SEU tolerant have been identified for listing under the ASAP. The ACQ/ACTQ quiet series of devices from National Semiconductor Corporation suitable for designers who require improved floor noise margins for critical circuit applications will be included in this section. In addition, information on low voltage (3.3)/low power

devices for mixed signal applications will be provided on-line.

The new technology section will include information on the Essential Services Nodes Module and the MONGOOSE processors developed by NASA/GSFC. These devices are available from Honeywell in Minneapolis.

The ASAP and the Passive Supplier Assessment Program (PSAP) are actively engaged in bringing on-line additional sites that are presently under construction for the NASA Parts Selection List (NPSL) which was put up on the web last year . The transistor section is due for release during the middle part of February this year. The NPSL can be accessed at http://misspiggy.gsfc.nasa.gov/npsl.

Mechanical Deflection System - A Low-Cost Fast-Response Alternative to Thermal Cycling

Tom Clifford
Process Specialist
Lockheed Martin Missiles and Space
(408) 742-6950
tom.clifford@1mco.com

ABSTRACT

Thermal-cycling, used in evaluation of reliability of CTE-mismatched SMT solder-joints, typically requires several months of expensive testing. An alternate method, developed by IBM, imposes cyclic shear by repetitive torsion of the SMT assembly. This Mechanical Deflection System (MDS) method typically takes a week or less. This paper reports an exploratory comparative study of the two methods. The results show similarities in failed components and in the specific failed joints, as well as in visual and microscopic appearance of the cracks. The MDS method shows promise: certain configuration factors could be evaluated for relative performance, but additional empirical and fundamental studies are necessary before MDS alone can be used to predict service life reliability. At that point, cost and time savings could be substantial.

INTRODUCTION

Thermal-cycle testing, properly done and interpreted, is a useful indicator of long-term reliability of CTE-mismatched SMT solder-joints. It is supported by twenty years of theoretical and empirical studies (Coffin-Manson, Englemeier, and recently many others) that link the mission duty-cycle, the physical configuration of the joint, the thermal-cycle test results, and the predicted life-time of the joint. Unfortunately, thermal-cycle test typically require several months of expensive testing resources. This often delays product development and hampers implementation of new technologies.

A new test method has been developed by IBM that might alleviate this problem. IBM calls it their Mechanical Deflections System (MDS)[1]. This device imposes a repetitive mechanical twist to the assembly, at selected temperature and cycle rates. This is said to simulate the cyclic shear regime that happens in CTE mis-matched joints during thermal cycling. The advantage is that MDS is much faster: days rather than weeks or months. The disadvantage of MDS at this point is that it is unproven, has little fundamental and empirical back-up, is geometry limited, and only crudely simulates the thermally induced cyclic-shear regime, which itself only imperfectly models the actual mission duty cycle. Comparisons between the two methods, as well as modeling and analysis, are needed to establish usable correlations between the two methods that could enable predictions of actual service life. An exploratory comparison study is reported below.

SUMMARY

The first step in evaluating the MDS concept was to demonstrate whether the cracks did, in fact, mirror those encountered with thermal-cycling. If the cracks look the same, and appeared in the same components, at the same joint locations, at the same relative severity, then we could conclude that the same mechanism was at work, and we could proceed with the method. If the pattern of cracking bore no resemblance to thermal-cycled crack patterns, then we must conclude that unknown effects were operating and there would be no reason to proceed further. A study was planned to test this hypothesis.

A group of SMT assemblies was identified as being well-characterized and representative of current technologies. Four of these assemblies were sent to IBM for MDS testing; other similar ones were held back and thermal-cycled in the Lockheed Martin Sunnyvale facilities. All these assemblies included components that would be expected to develop solder joint cracks under extended extreme thermal-cycling conditions.

The samples were tested at IBM under conditions selected by IBM to be most appropriate for these samples, to develop representative cracks at severe easily documentable levels. The parameters were 100°C, 0.4 degrees of twist per inch of board length, 2 minute cycle (15 sec ramp + 45 sec dwell), for 20,000 cycles. The length of MDS cycling was arbitrarily extended beyond the typical one week, to be sure that severe, easily documentable solder fillet cracks would develop. The thermal-cycling profile was -55°C to +125°C, 30 minute dwell at each temperature, with transitions @ 5°C / min, approximately 1000 cycles for a total cycle time of ~ 2.2 hours.

Cracks in the MDS specimens' solder fillets were observed on the largest components, at the corners. The occurrence of these failures: largest components, at the corners, were identical to positions of failures seen in thermal cycling.

MDS fillet crack locations (cracks at the heel of and toe fillets of the solder joint, and precursor cracks along the sides) are identical to the failure locations seen in thermal-cycled failures.

MDS crack morphology (crack location within the solder fillet, appearance of solder grain structure, as seen in microscopic x-sections) are visually identical to the cracked morphology seen in thermal-cycled failures.

The components' solder fillets that would not be expected to fail, based on thermal cycling experience, in fact did not fail in the MDS testing. These included small J-lead and gull-wing parts, passives, and the center leads of large gull-wing and J-lead components.

This study confirms that the MDS cyclic exposure produces failure patterns and failure modes that are very similar, if not identical, to thermal cycle experience, over a range of common SMT components. The two methods provide the same discrimination, regarding types of components and solder joint locations within a component. The test time is substantially shorter with the MDS approach.

However, this study was not extensive enough to justify recommending that MDS should completely replace thermal-cycling. We have not established a numerical equivalence between MDS and thermal cycling, and certainly no relationship between MDS data and failures of actual hardware under mission conditions. This will require additional empirical and fundamental studies, and larger sampling.

CONCLUSIONS

MDS appears useful for comparison of closely related configuration variables, for which there are documented thermal-cycle or in-service reliability data. MDS could probably correctly evaluate the effects of variations in component size, solder joint and fillet configuration, lead material, adhesive support, positioning registration and other mechanical factors. At this time, it could also be used for comparing a new-design assembly with a previously qualified similar-design assembly, wherein the above factors are the only differences.

At this point, MDS methodology alone cannot be used to arrive at an absolute reliability lifetime value, and it cannot be casually used for material evaluations that center on CTE and / or stress-relaxation effects (different solder alloys or board materials, comparing SMT with BGA packages, variations in temperature excursions, etc.). Additional comparative studies should be considered, as developments proceed in advanced electronics packaging and mounting, or if extensive thermal-cycling tests are considered for current technologies. These studies would need to be backed up by modeling and theoretical analyses.

DETAILS

Thermal cycling will cause cracking in CTE mismatched solder-joint fillets, after a number of cycles, depending on the materials, joint geometries, and the thermal cycle profile. These results can be used to estimate service life, using analytical modeling which is beyond the scope of this paper. Typically, the thermal-cycle activity is used to validate models or to explore new geometries, but the length of time required to accumulate useful data can

be a real barrier to qualification; or in its absence, can limit the accuracy of life estimates. Indeed, without the appropriate data, an over-conservative (more expensive, bulky, etc.) configuration might be specified in order to ensure reliability. Better models and analytical methods are being developed, but clearly, a faster method of simulating CTE -induced fatigue in actual hardware should be useful. The first step in this effort, regarding the MDS system of IBM, was to set up a back-to-back series to demonstrate, in a crude empirical way, that the cracks look the same.

The number of cycles was set to be sure that cracks developed. The usual discussions on the definition of "failure" (i.e., little cracks…, big cracks…, refereed cracks…, toe-plus-heel cracks…, completely loose cracks…, electrically open at rest cracks…, open for a certain number of milliseconds cracks… >30 ohm cracks …, 10% or 3X increase in resistance cracks…, "persistent" cracks… etc.) were waived for this purpose. Pass or failed judgments were inappropriate for this exercise: only a careful comparison of any resulting cracks needed to be made.

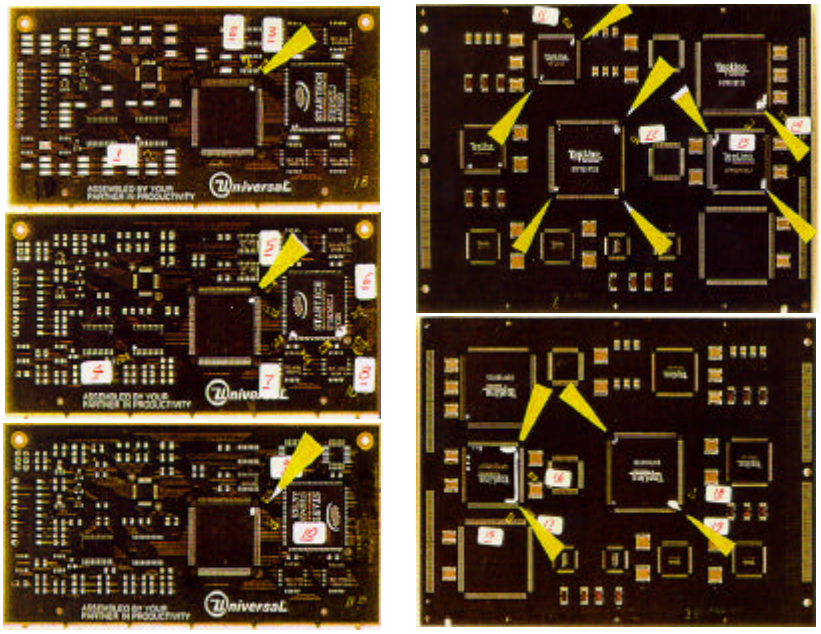


Figure 1

Figure 1 shows the boards submitted for MDS testing. These include three 3" X 6 " Universal® Glass/Epoxy panels, plus one two-sided 6" X 8 " SMT board.

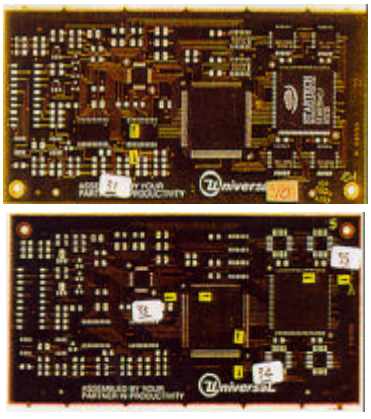


Figure 2

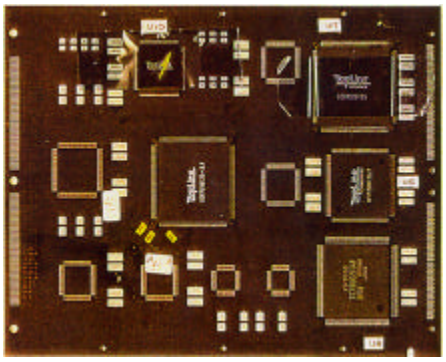
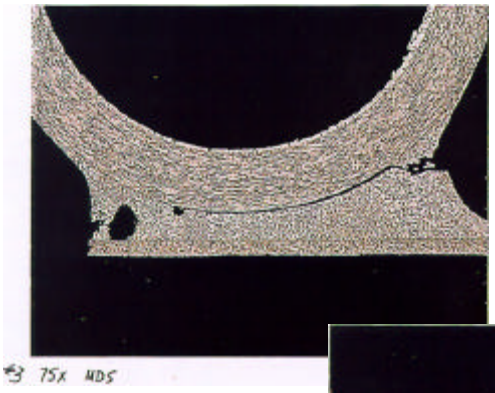


Figure 3

Figures 2 and 3 show the equivalent boards held back for thermal cycling (-55°C to +125°C, 30 minutes dwell, 5°C/minute transitions, ~ 1050 cycles).

Note, in the MDS-tested specimens in Figure 1 the specific solder fillets observed to be cracked, are indicated by the large arrows. Note similarly, in the thermal-cycled specimens in Figure 2, the solder joints observed to be cracked, marked by the arrows. It is obvious that both methods tend to cause cracks in the largest components, at the corner joints as expected, based on expectations gained from thermal-cycle experience.

Figure 4 shows an example of a cracked J-lead fillet from the MDS series, joint #7; and a cracked J-lead fillet on the similar component from the thermal-cycle series, joint #35.



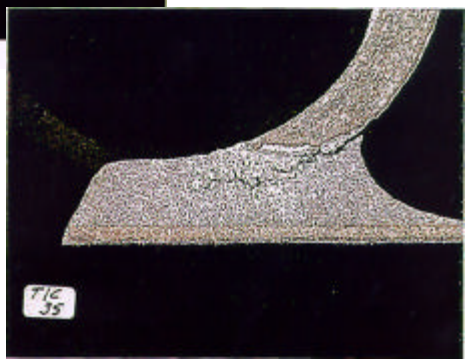
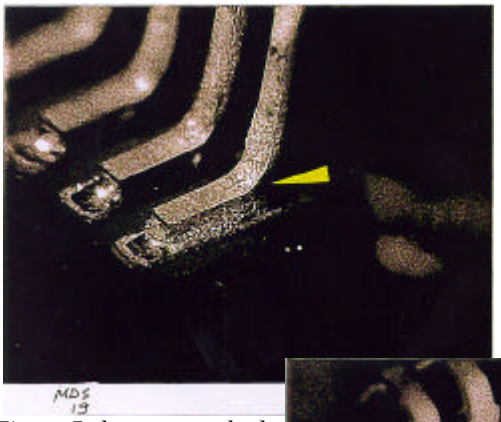


Figure 6 shows a cross-section of a typical failed J-lead from the MDS series, joint #3; and an equivalent failed J-lead on the similar component (although cut off-axis in the pot-n-polish process) from the thermal-cycled series, joint #35.



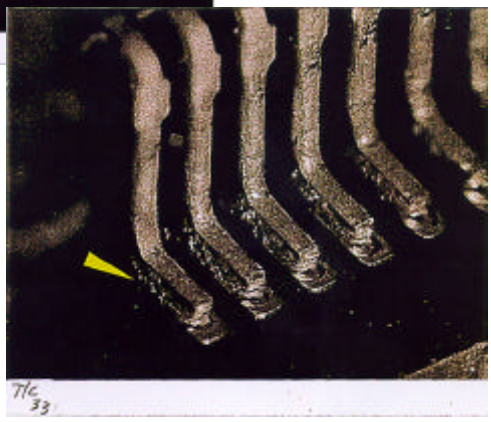
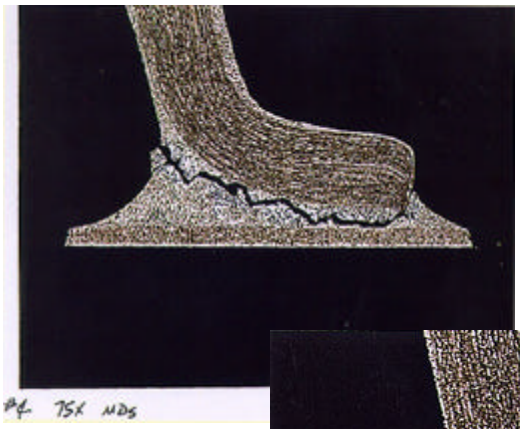


Figure 5 shows a cracked gull-wing solder joint from the MDS series, joint #19; and an equivalent cracked gull-wing joint on the similar component from the thermal-cycled series, joint #33



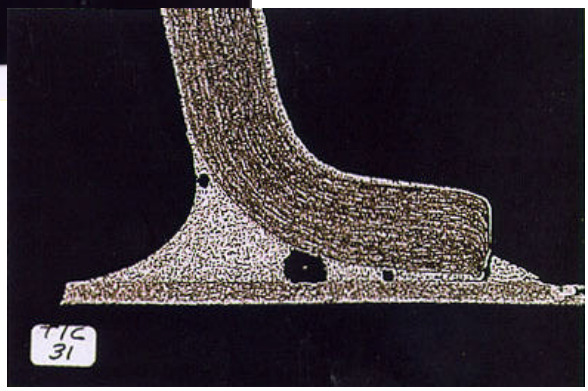


Figure 7 shows a cross-section of failed gull-wing solder joints from the MDS series; joint #1 and #4; and an equivalent failed gull-wing joint on the similar component from the thermal-cycled series, joint #31.

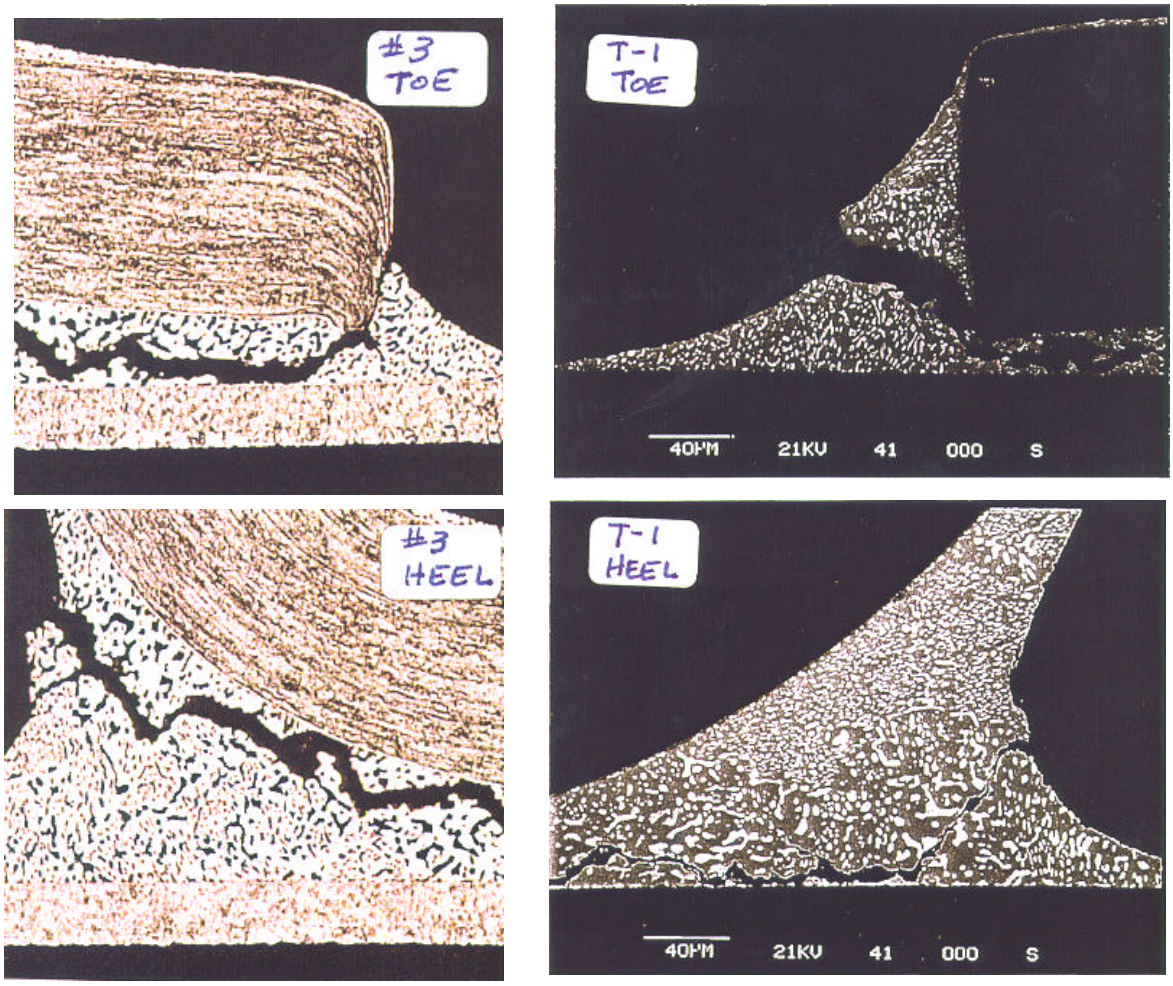


Figure 8 shows higher-magnification shots of a typical cracked gull-wing joint #3 from the MDS series, and an equivalent joint # T-1 from the thermal-cycle series. The crack morphology appears quite similar.

The observations in Figure 8 document only visual similarity in crack development (component, lead position, location of the crack on the fillet, metallurgical morphology) between the two methods. All this strongly suggests that the failure modes and mechanisms are essentially equivalent, under these conditions. No quantitative correlations nor specific time savings were explored in this study. The MDS test duration of 28 days was selected, at the request of the author, to ensure extensive cracking, severe enough for easy photography. Stopping the test much sooner would have shown some failures, perhaps equivalent in severity to the 1000 thermal-cycle controls. In any event, substantial time savings appear to be realizable. The test report from IBM[2] mentions some savings and details on relative crack development among types of solder joints. The current work was intended to document equivalence in failure mechanism, potential cost and time-savings, feasibility for current application; and identification of future work. This has been accomplished.

The author acknowledges the support of Alex Zubelewicz at IBM, the developer of the MDS system; as well as the SMT crew at the Lockheed Martin Missiles & Space, Sunnyvale facility: particularly Yun Wang for sample assembly, Tom Cox for micro-photography documentation, and Jim Springmeyer for providing resources for this study.

1 Zubelewicz "MDS … an Innovative Test Method for SMT Assemblies" Interpak 95

2 Test Report, IBM to Lockheed-Martin, April 25, 1997. Available on request from the author.

Reliability of Chip Scale Packages

Dr. Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
California Institute of Technology
Tel: (818) 354-2059
email: Reza.Ghaffarian@JPL.NASA.Gov

INTRODUCTION

Emerging Chip Scale Packages (CSPs) are competing with bare die assemblies and are now at the stage Ball Grid Arrays (BGAs) were about two years ago. These packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages. Availability of board solder joint reliability information is critical to the wider implementation of Chip Scale Packages (CSPs). This paper will compare three different CSP concepts as well as their assembly reliability.

CHIP SCALE PACKAGES

CSPs are defined as packages that are up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Many manufacturers now refer to CSPs as packages that are the miniaturized version of their previous generation. Two concepts of CSPs are shown in Figure 1.

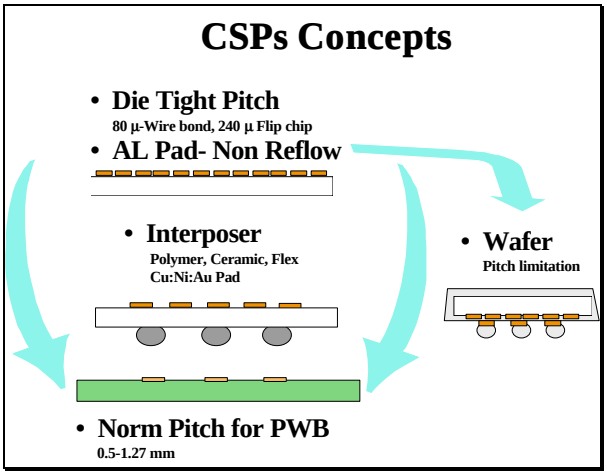


Figure 1: Two Chip Scale Package Concepts

CSP ASSEMBLY RELIABILITY

Currently, most data has been generated for package qualifications by manufacturers, with very limited published information available on assembly reliability. This data is of limited value to the end user since it has often been collected under significantly different manufacturing and environmental conditions or for packages with different pin counts.

Failure at the board level could be caused by either the failure of the package itself or the package to board connection. The latter could be caused by the intrinsic wear-out mechanisms or by hostile environmental factors. The thermo-mechanical wear (creep) of solder joints is the cause of failure for most CSP assemblies. Failure of a solder joint can be the result of mechanical stresses in a non-uniform thermal expansion and / or by contraction of different materials in the assembly. To achieve the least damage to solder joints, thermal mismatch between the die and board should be minimized either by package optimization or by appropriate board material selection in order to closely match the coefficient of thermal expansion (CTE) of the package. Only a few of the CSP packages have been designed to alleviate damage due to the thermal expansion of package / board mismatches.

LITERATURE DATA ON CSP ASSEMBLY RELIABILITY

Table 1 lists the assembly reliability for flex or rigid interposers, and wafer level packages. Aspects of cycling conditions with their failure mechanisms are summarized in the following:

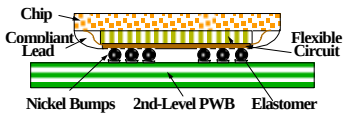
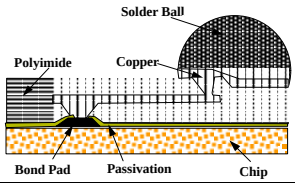
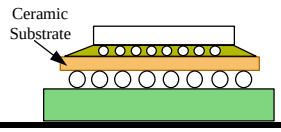
CTE absorbed CSP: Thermal cycling test results for a CTE-mismatched relieved package are shown in Table 1. This package uses TAB-like IC interconnects, a resilient elastomeric interposer, and eutectic solder balls. The resilient interposer in conjunction with the springiness of TAB interconnection reduce thermal expansion differences between the chip (CTE 2-3 ppm / °C) and PWB (CTE for FR-4 ~15 ppm / °C). This package has been shown to be reliable, robust, with no requirement for underfilling. Thermal cycling / shock data given in the Table were for daisy chain packages on FR-4 and were performed from the liquid nitrogen temperature (-196°C) to hot oil (160°C). Because of the low strain state of solder joints, fatigue failure mechanisms of solder joints were not observed and failures shifted to the heel of the TAB interconnection with high mismatched stress levels. Significant improvement was observed when ductile gold leads were used. The gold version showed no failure up to 2000 cycles in the range of -65°C to 150°C. The thermal cycling screening test

results associated with assembly exposures to extremely low (stress conditions) and high temperatures (strain conditions) are not realistic and therefore their failure mechanisms may not be representative of field failures. One such failure, due to extreme high temperature exposure, is the chambering and deformation of FR-4 close to its glass transition temperature (Tg). PWB materials will show severe damage if the cycling temperature becomes close to or exceeds their glass transition temperature (the temperature that polymer materials start to become soft). Indeed, it was observed that FR-4 plated through holes had massive barrel cracking failures in the -65°C to 150°C temperature cycling range.

Wafer packages with extreme CTE mismatch: Thermal cycling test results for assembly of a wafer redistributed package is shown in Table 1. In this package, a thin film metal/polymer redistributes the location of the solder bumps over the chip to make these compatible with the surface mount footprint.

The height of the package type increases by the thickness of the metal polymer layer from the bare chip. This additional layer will not generally absorb the CTE mismatch between the chip and board and therefore the assembly reliability of this package is expected to be very similar to the C4 assembly. Without underfill materials, the assembled package failed in less than 40 cycles when subjected to thermal cycling between 0°C and 100°C. For these types of packages, underfilling is usually required to achieve an acceptable level of assembly reliability. The underfilled assemblies did not fail up to 2,000 cycles. Ceramic packages with rigid interposer: The non-wafer level ceramic packages have shown reasonable assembly reliability with no underfilling. Thermal cycling results for a ceramic package on FR-4 are also included in the Table 1. The ceramic CSP uses the same design rules as multilayer ceramic (MLC). The first level interconnection choices of thermal compression and sources is precipitation of host atoms that result in an elevation in pulse threshold current (driving current gold stud bump, solder flip

Table 1. Literature Data on CSP Assembly Reliability

Package Type Schematic (not to scale)	Cycling Condition	Total Cycles	Fails/ Samples	I/O	References (comments)
Flex Interposer CTE matched 	-196°C<>160°C -65°C<>150°C	130 no underfill 1163 2000*	0/3 0/46 0/34	188 188	J. Fjelstad, T. DiStefano, B. Faraji, C. Mitchell, z. Kovac, "mBGA Packaging Technology for Integrated Circuits," *NEPCON East*, June 1995 T. DiStefano, J. Fjelstad, "Chip-scale Packaging meets future design needs,"*Solid State Technology*," April 1996 * Gold bond ribbon. Ducticle-copper bond ribbon survived 500 cycles.
Wafer Level Redistribution 	0°C <> 100°C (Thermal Shock)	>2000 underfill <40 no underfill	NA	266	R. Chanchani, et al, "mini Ball Gird Array (mBGA) Assembly on MCM-L Boards," *Proceedings of Electronic Components and Technology Conference*, May 18-21, 1997
Ceramic CSP 	-40°C <>125°C	~600* no underfill, PWB 0.6 mm >900* no underfill, PWB 1.6 mm	NA	220	R. lanzone, "Ceramic CSP: A Low Cost, Adaptive Interconnect, High Density Technology," *Proceedings of second International Conference on Chip Scale Packaging, CHIPCON* '97, Feb. 20-21, 1997 *Private Communication

chip, and wire bond.) The strength, rigidity, coplanarity, and chamber of the package are excellent. The package assembly on a 0.6 mm low Tg FR-4 failed at about 600 thermal cycles between -40°C to 125°C. Cycles to failure increased to more than 900 cycles when PWB thickness increased to 1.6 mm. Thicker FR-4 is expected to show better rigidity when exposed to 125°C, temperature close to the low Tg FR-4 polymer used for this study.

SYSTEMATIC APPROACH TO ASSESS CSP BOARD RELIABILITY

Board reliability information is a key element in facilitating CSPs implementation in commercial and especially in high reliability applications. For wider applications of this technology, the potential user will need design reliability data since often they do not have the resources, time, or ability to perform complex environmental characterizations. To help build the infrastructure in these areas, JPL has formed a consortium with the objectives of addressing systematically many technical issues regarding the interplay of package type, I/O counts, PWB materials, surface finish, and manufacturing variables for the quality and reliability of assembly packages. Understanding the philosophy of testing to meet system requirements as well as detecting new failure mechanisms associated with these miniaturized packages is the key to collecting meaningful test results.

The JPL-led microtype BGA consortium with more than twenty team members is now building its first test vehicle with fifteen packages from eleven manufacturers with I/Os ranging from 12 to 540.

REFERENCES:

Ghaffarian, R. "Micro-BGA Quality and Reliability Development Plan," EEE Links, Vol. 3, No. 1, March 1997

ACKNOWLEDGMENT:

The research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

Capabilities and Reliability of LEDs and Laser Diodes

Melanie Ott
Technology Validation Assurance Group
Swales Aerospace
NASA Goddard Space Flight Center
301-286-0127
melanie.ott@gsfc.nasa.gov
updated 9/3/97

In general, high temperature testing is used to determine LED and laser diode lifetimes, even though laser diode failure mechanisms are more sensitive to increases in current density. As a measured parameter of degradation, the current density is of great significance when searching for failure modes in a laser diode. Raising the current density however, is not really indicative of lifetime since it is more likely a situation to be avoided than one that simulates normal lifetime degradation. The reliability of semiconductor sources is very dependent on the degradation modes. This report intends to summarize some of the degradation modes and capabilities of typical LEDs and laser diodes currently used in many communication and sensing systems.

LED's are typically used in multimode transmission systems where data rates no larger than 50 Mb/s are required. They have larger spectral widths and can add to the problem of dispersion in communications systems. Laser diodes are used in systems that require coherent and often single mode light such as high data rate communications and sensing applications. In comparison to laser diodes, LED's can generally be driven harder, are less expensive, have lower power, have larger emitting regions, and longer lifetimes. Lasers, unlike LED's will not operate below a threshold current. Meaning, only when the threshold current is reached will the diode commence lasing (functioning).

As mentioned previously, LEDs and laser diodes are temperature sensitive when considering overall lifetime, for example, operating a laser diode at 10 °C higher than rated will half the life of the diode. Also a laser usually will stop functioning at 100°C. The degradation modes that result in failures or gradual degradation of these devices can be modeled using Arrhenius relationships where each degradation mode carries a specific activation energy. For example in reliability tests in which lifetime is based

on temperature aging the relationship is life = A $e^{Ea/kT}$.

CAPABILITIES:

Table 1 summarizes available information on a wide range of LEDs and laser diodes. Specialty devices are not included in this summary and the parameters specified are highly generalized. This data is included as a reference when considering which device, due to attribute or parameter, is most useful for the application.

DEGRADATION MODES

The main degradation modes are: dislocations that affect the inner region, metal diffusion and alloy reaction that affect the electrode, solder instability (reaction and migration) that affect the bonding parts, separation of metals in the heat sink bond, and defects in buried heterostructure devices. These modes are enhanced by current during ambient temperature operations. Facet damage due to oxidation is enhanced by light or moisture and is particular to laser diodes.

DEGRADATION OF THE INNER REGION:

Point Defects lead to Dark Line Defects

The main cause of degradation in the inner region is directionally dependent on the crystal structure as well as dependent on the material used for the source. In particular, dislocations along the 100 direction grow as a result of interstitial atom or vacancy point defects. AlGaAs/GaAs show a much higher rate of dislocation growth than sources fabricated in InGaAs(P)/InP. In general, the longer the wavelength response of the material, the less sensitive it is to this point defect. Point defects can also lead to a slow degradation or a rapid degradation when the defect leads to a plane defect in the crystal structure. Improving crystal growth techniques is the only way of making them less likely.

Table 1: Comparison of Typical Parameters of Interest for LEDs and Laser Diodes

Attribute/ Parameter	LEDs	Laser Diodes
Radiative Recombination	Spontaneous Emission	Stimulated Emission
Particle Phase	Incoherent	Coherent
Polarization state	Randomly polarized	linearly polarized
Direction	Random	linear
665 nm	GaAsP	GaAlAs
800-930 nm	Ga_{1-x} Al_xAs	Ga_{1-x} Al_xAs
1300, 1550 nm	InGaAsP	InGaAsP
Spectral Width	$\Delta\lambda \approx 1.45\ \lambda^2$ kT λ in μm, kT in eV, k = Boltsman's constant, T = junction temp	
Spectral Width, GaAlAs	10s of nm	< 1.5 nm
Spectral Width, InGaAsP	surface emitting, 100 nm edge emitting, 60 -80 nm	.1 to 10 nm
Significant Parameters	BW vs Power BW increases at the expense of power	Threshold current, Index guided: 10 to 30 mA Gain guided: 60 to 150 mA
Reliability lifetimes	10^5 to 10^8 hours	10^5 hours
Temperature Effects	increases wavelength by .6 nm/ °C	wavelength varies by .25 nm/°C threshold current rises by .5mA/°C
Rise Time	1 to 100 ns	< 1 to 10 ns
Output Power	10 - 50 (high power) μW	1 - 1000 mW
Modulation	3 Mhz - 350 Mhz	> 350 Mhz

In general the bandwidth-rise time relationship is calculated as BW = .35 / rise time.
x is between 0 and 1 in Ga_{1-x} Al_xAs

Other Types of Dark Line Defects

Dislocations along the 110 crystal axis will grow and form as a result of mechanical bond stresses. The result of these types of dislocations are Dark Line Defects (DLD) and induce rapid degradation of the device. Another degradation in InGaAs(P)/InP sources is precipitation of host atoms that result in an elevation in pulse threshold current (driving current required for lasing). The higher this current is driven, faster degradation of other mechanisms as well as dark line defects, will occur. In looking for these types of degradation mechanisms it is more revealing to monitor the threshold current as opposed to the output power. The threshold current is more sensitive to defects than the output power. As the current is driven to saturation, noise will develop in the laser signal.

SURFACE DEGRADATION

Facet Damage From Oxidation in Laser Diodes

Oxidation of a source facet can lead to slow degradation. Sources that contain higher concentrations of aluminum tend to inhibit the oxide growth. Aluminum particles are active and inhibit diffusion to the facet by decreasing the junction temperature. AlGaAs/GaAs sources will develop oxide thickness proportional to their output power levels when operating at low power and will grow thickness proportional to the square of the output power levels when operating at higher power levels.

Catastrophic Optical Damage (COD)

COD occurs as a result of facet melting due to current concentration and optical absorption. Optical absorption that encourages nonradiative recombination results in heating and melting at the facet. The heat generated will also cause the bandgap to shrink, and as a result, the current concentration increases creating more heat and the cycle continues.

The AlGaAs/GaAs sources are much more sensitive to this type of damage than the InGaAs(P)/InP sources. Where the first is considered unstable against oxidation and has high rates of facet oxidation, the second has a much lower rate of oxidation with respect to time and output power. The same is true for COD as the first will experience this at levels less than 1 MW/cm^2 the second will not experience until power densities of tens of MW/cm^2 have been reached. One solution to this is a non-absorbing mirror structure or NAM. This technology is under development, but it is difficult to manufacture at present.

Alloy Electrodes

In sources (and photodetectors) with alloy electrodes, degradation develops as a result of the metal diffusing in towards the inner region. One example of an alloy type electrode is AuZnNi. During operation the metal will diffuse creating spikes along with the direction of current flow. The result is dark spot defects in the inner region of the semiconductor. The Schottky-type electrodes such as Ti/Pt/Au do not seem to cause the same degradation. The metal forms an inert interface between the electrode and the semiconductor surface.

Bonding Parts

Soft-solders can reduce mechanical stresses on the bonding surface but tend to add to early degradation of the device. In, Sn, and Sn-rich Au-Sn are among the type of soft (low melting point) solders that are attributable to solder instabilities like whisker growth, thermal fatigue, void formation at the bonding part, and diffusion similar to what occurs with the alloy electrodes when in contact with the semiconductor surface. These instabilities directly lead to sudden premature failures. The higher melting point solders, or hard solders, which include such materials as Au-rich AuSn eliminate many of the instabilities that plague devices that have problems with soft solders.

Buried Heterostructure

In Buried Heterostructure diodes (BH), the configuration and index of refraction changes. Nearby, the active region of the laser diode creates a waveguide for light emerging from the interactions. This type of laser is considered an “index-guided” laser. The n-type InGaAsP active emitting region is surrounded on both sides by the p-type InP. The degradation mode in these lasers is associated with a breakdown or degradation of the active region due to a decrease in injected carriers. The degradation of the BH interface is considered a wear out failure and is not a sudden type failure.

Above is a summary of the most generally common characteristics and degradation modes of laser diodes and LEDs. Facet degradation is specific to laser diodes. Some degradation modes can be eliminated

through redesign of the semiconductor structures or through packaging techniques. For more information please review the references at the end of this paper.

Reliability Equations:

There are several methods of extrapolating source lifetime including methods of calculating lifetime given power output operating temperature, device drive currents, and decrease in output power. Below are several of the extrapolation equations for predicting source lifetime.

Output Power:

The lifetime of a laser diode or LED can be approximated by the following relationship. Given an initial power output of the device P_o and the exponential lifetime τ, the power output over time t, can be extrapolated.

$$P_{out}(t) = P_o e^{-t/t}.$$

Assume that for a given time t, the power output of the device has dropped to a percentage from the initial power level such that Power ratio, $P_R = P_{out}/P_o$ and solve for t such that,

$$\tau = -t / \ln(P_R).$$

Now with t known, as well as the initial power output P_o, the power output $P_{out}(t)$ can be extrapolated over time t.

Drive Current:

Another way of predicting source lifetime is by extrapolation of the current density. Elevated currents can bring out many of the degradation mechanisms associated with point defects in devices such as AlGaAs. If J is defined as the current density, the lifetime of the device is defined as t, and the empirical value parameter is defined as n, then there exists a relationship such that $t \propto J^{-n}$. Therefore if the lifetime of the device, t_o is known for a given operating current, I_o then a relationship between drive current and device lifetime can be deduced from

$$\frac{t_o}{t_2} = \frac{J_o^{-n}}{J_2^{-n}} = \left(\frac{J_o}{J_2}\right)^{-n} = \left(\frac{I_o}{I_2}\right)^{-n}.$$

Solving for t_2 such that a relationship exists where lifetime can be predicted as a result of elevated or decreased operating drive current, I_2.

$$t_2 = t_0\left(\frac{I_2}{I_0}\right)^{-n}.$$

The values of n range from 1.5 to 2.0, with the larger n indicating more of a reduction in operational lifetime or greater sensitivity of the device to increased currents.

Temperature:

For determining the relationship between temperature of the device to predict lifetime an Arrhenius relationship can be expressed as,

$$t = ce^{Ea/kT}$$

where

E_a is the activation energy for the device in units of eV,

k is Boltzman's constant = $1.38 * 10^{-23}$ Joules / Kelvin,

T is absolute temperature, (273.2 + °C) in units of Kelvin,

c is the device constant in units of time, and

e is electron charge = $1.6 * 10^{-19}$ joules / eV.

The lifetime in this relationship is defined as unexceptable drive currents for lasers where the drive currents elevate to 1.2 to 1.5 times the rated drive current and for LEDS can be output power loss below that of the rated value due to point defects. For life time versus temperature calculations the following E_a, activation energies can be used:

AlGaAs / GaAs lasers ~ .7 eV

AlGaAs LEDs ~.5 eV

InGaAsP / InP (longer wavelength) ~ .16 eV

InGaAsP / InP Buried Heterostructure ~ .9 eV

GaAlAs Double Heterostructure LED ~ .56 eV.

Given a known activation energy E_a, operating temperature T_o and lifetime of the device t_o, the constant can be calculated by

$$c = t_o e^{-Ea/kT_o}.$$

Or as a ratio, t_2 can be solved for in terms of T_2 given T_o and t_o such that

$$\frac{t_o}{t_2} = \frac{e^{Ea/kT_o}}{e^{Ea/kT_2}}.$$

Simplifying to solve for t_2 as a function of the temperature for accelerated life testing,

$$t_2 = t_o e^{-\frac{Ea}{k}\left[\frac{1}{T_o}-\frac{1}{T_2}\right]}.$$

Note that for photodetectors the degradation mechanisms are different but the same Arrhenius relationship can be used to determine lifetime of the device given different operating temperatures. The same relationship holds with the activation energy being ~ .7 eV for infrared detectors. Also it is important to note that the criteria for detector lifetime degradation is based on receiving an unacceptable signal to noise ratio output as a result of the accelerated temperature life test.

References

1. Mitsuo Fukuda, "Semiconductor Laser and LED Reliability," OFC Tutorial 1996, San Jose, California.
2. Mitsuo Fukuda, "Laser and LED Reliability Update," Journal of Lightwave Technology., vol.6, pp.1488 - 1495, 1988.
3. Mitsuo Fukuda, "Degradation Modes of Semiconductor Lasers used in Optical Fiber Transmission Systems," SPIE vol. 1634, pp. 184-191, 1992.
4. John P. Powers, *An Introduction to Fiber Optic Systems*, Aksen Associates Inc.,1993.

Methodology for Structural Integrity Assessment of High-Density Microelectronic Devices and Components

Dr. E. James Chern
Goddard Space Flight Center
(301) 286-5836
jim.chern@gsfc.nasa.gov

DESCRIPTION:

Advances in electronics, computer and manufacturing technologies have enabled many industries to significantly reduce the size and weight, and improve the performance of their products. NASA is gearing towards using miniature spacecraft and systems for its planetary, space science and Earth science studies. To meet the challenge of smaller, better, cheaper and faster space flight missions, NASA is developing and implementing advanced microelectronic components and devices for next generation space flight applications. Micro-Electro-Mechanical Systems (MEMS), micron scale sensors and actuators fabricated typically from silicon wafers using micro machining techniques, have shown promises as a prime candidate for use in miniature space flight systems. Advanced Commercial-Off-The-Shelf (COTS) high-density packages and processes such as micro-ball grid array, flip chip assembly and plastic-encapsulated microcircuits, are also potential sources for next generation space flight systems. However, in order to be qualified for space applications, the MEMS and COTS components and devices have to sustain harsh launch conditions such as high-g load and random mechanical vibration, and hostile service environments such as radiation and temperature excursions.

Joint interface integrity of MEMS and COTS devices such as bonding of cantilevers to substrate, frames to substrate, stacking seals, chips to substrate, heat sinks to substrate, lid seals, wafer assemblies, die attachments, and interconnects are extremely critical to the function and service lives of the devices. Due to their ability to penetrate the material, ultrasonic techniques are the most commonly used nondestructive evaluation (NDE) method for evaluating bonded joint integrity. The scanning acoustic microscope, which operates at high frequency (50 to 100 MHz) is capable of imaging

bonds at depths of up to several millimeters, revealing detail that is not discernible with other conventional NDE techniques. However, because the layers of these microdevices are principally micrometer-scale components, the signals of interest are often superimposed with signals of other features. Structural integrity of the interface is thus very difficult to determine. In this article, we identify a time-gating approach to enable the examination of critical bonds with an improved scanning acoustic image.

For standard ultrasonic C-scan applications, the entire reflected pulse of the area of interest is gate-peak-detected to produce the ultrasonic image. The time response of the various interfaces of a multilayered structure can be expressed as

$$T(k_i, k_2, ..., k_n) = \sum_{i=1}^{n} k_i t_i$$

where n is the number of layers, $k_i = 1, 2, 3, ...$ and $t_i = 2d_i / v_i$ is the time it takes the pulse to make a round trip, traveling through ith layer thickness d_i with a wave velocity of v_i. Although the time of occurrence can be easily calculated, the reflected pulses from various interfaces are not distinctly isolated. The pulse of interest is typically modified by other signals. When the width of the timing-gate is set to encompass the entire pulse envelope of the signal of interest, the resolution of the image is compromised. It is observed that by limiting the gate width to include only the very cycle of the signal of interest, the sharpness of the acquired ultrasonic image is greatly improved. The integrity of the specific joint interface can be obtained and analyzed. Other hardware enhancements such as sensors and drive-pulse shaping, can also be instituted to improve the signal to noise ratio. As a revolutionary improvement of the system, we propose the approach of using a phase-lock loop to track the peak pulse of the signal of interest. This method can dramatically enhance the capability of the system to encompass a variety of complex structures. This improved scanning acoustic microscope system, when fully instituted, will have extensive applications to spaceborne as well as commercial microelectronic devices.

Low Dose Rate Total Ionizing Dose (TID) Evaluation of Bipolar and CMOS Parts Used in SMEX, MIDEX, GOES, and HST Projects

Kusum Sahu
Unisys Corporation, Lanham, MD
(301) 731-8954
Kusum.K.Sahu.1@gsfc.nasa.gov
Scott Kniffin
Unisys Corporation, Lanham, MD
(301) 731-8649
Scott.D.Kniffin.1@gsfc.nasa.gov

In 1997, a large number of commercial process microcircuits and semiconductor devices were tested for TID radiation effects to determine their suitability for use in several NASA programs. The devices cover a wide range of functions including frequency to voltage converters, demodulators, power MOSFETs, operational amplifiers, ADC / DAC's, voltage references, various memory devices, transistors, etc. The manufacturer provides no radiation hardness guarantee for these commercial process devices. The objective of these low dose rate characterization tests was to determine the suitability of these parts in various NASA programs with different TID requirements. These requirements varied from 5 to 200kRads(Si) depending on the orbit, mission duration, shielding, location of the parts in the spacecraft / instrument box, and other factors.

TID testing was performed using a Co-60 gamma irradiator in the Radiation Effects Facility of NASA's Goddard Space Flight Center. All parts were from the flight lot and had the same LDC. During radiation testing for each device lot, four to eight parts were irradiated at room temperature (25°C) under static bias conditions and one or two parts were kept as unirradiated control samples. The most commonly used dose steps were 2.5, 5, 10, 15, 20, 30, 50, 75, and 100kRads(Si). The dose rate for the testing varied from 0.01 to 0.1 Rads (Si) / s depending upon the part type and the dose step. Generally, the dose rate of 0.01Rads / s is used for TID steps up to 10 kRads and a higher dose rate of 0.05 to 0.1Rads / s is used for total dose steps greater than 10 kRads. After the final irradiation step, the parts are annealed under bias at room temperature (25°C) for periods ranging from 96 to 600 hours. The extended room temperature annealing (>168 hours) was performed when the parts

degraded significantly to determine if they would recover in the low dose rate space environment. After this room temperature annealing, some parts (CMOS technology) received an additional high temperature (100°C) annealing to detect any rebound effects.

Table 1 provides a summary of TID tests results for all part types tested in 1997. The radiation response of these parts varied significantly over the full range of exposure levels. Some devices showed no significant degradation and stayed within the pre-irradiation specification limits up to 50 to 100 kRads. However, many other devices (CMOS, Bipolars, MOSFETs) started to show degradation from the specification limits at very low radiation levels of 2.5 to 20kRads. However, for many part types these degradations from the specification limits were marginal (<10-20% of the pre-irradiation specification limits). In many cases, the application of these parts is such that some degradation from the pre-irradiation specification limits may be tolerable in the circuit application. The initial degradation level that we have listed in Table 1 is the radiation exposure level where one or more parts exceeded the manufacturers pre-irradiation specification limits. The significant degradation is the level where, in our opinion, the parts showed significant deviation from the specification limits. The details of the degradation for different test parameters are provided in the individual report for each part type. It is essential that designers review the details of the degradation for all test parameters before making a decision on the use of the part for the application.

The details of low dose rate TID characterization results and test procedures are provided in the PPM reports listed in Table 1. A copy of these reports can be obtained from the OFA Library at GSFC by calling (301) 286-7240.

Table 1: Low Dose Rate TID Test Results for Parts Tested in 1997 /1 /2

S/N	Generic Part No.	Part Type	Package Type	Mfr.	Test Level, krads(Si)	Init. Deg Level, /3 krads(Si)	Sig. Deg Level, /4 krads(Si)	LDC /5	Report
1	AD9050	10 bit Flash ADC	28 Pin DIP	AD	2.5-100	5	20	9615	PPM-97-036
2	AD570	8 bit ADC	18 Pin DIP	AD	5-50	>50	>50	9617	PPM-97-018
3	AD667	12 bit ADC	28 Pin LCC	AD	2.5-50	100	>100	9641	PPM-97-050
4	AD630	Demodulator	20 Pin LCC	AD	2.5-100	75	>100	9617	PPM-97-056
5	AD652	Freq. Converter	20 Pin LCC	AD	5-100	5	100	9434	PPM-97-057
6	OP470	OP AMP	28 Pin LCC	AD	2.5-50	15	30	9529	PPM-97-035
7	OP77	OP AMP	20 Pin LCC	AD	2.5-50	15	50	9525	PPM-97-031
8	OP497	OP AMP	20 Pin LCC	AD	2.5-50	5	30	9438	PPM-97-028
9	OP271A	OP AMP	20 Pin LCC	AD	2.5-50	10	30	9624	PPM-97-022
10	OP467	OP AMP	14 Pin LCC	AD	2.5-50	2.5	30	9647	PPM-97-021
11	OP27	OP AMP	8 Pin Can	AD	2.5-50	30	50	9648	PPM-97-019
12	OP400AY	OP AMP	28 Pin LCC	AD	2.5-30	2.5	10	9614	PPM-97-013
13	OP420RC	OP AMP	20 Pin LCC	AD	2.5-30	2.5	10	9617	PPM-97-012
14	AD624	Voltage Reference	16 Pin DIP	AD	2.5-50	10	30	9609	PPM-97-024
15	AD624	Voltage Reference	16 Pin DIP	AD	2.5-50	10	30	9608	PPM-97-023
16	AD580	Voltage Reference	TO-5	AD	5-50	>50	>50	9626	PPM-97-016
17	REF-43B	Voltage Reference	20 Pin LCC	AD (PMI)	2.5-100	10	>100	9536	PPM-97-032
18	AD562	12 bit DAC	24 Pin DIP	AD/PMI	2.5-125	50	75	9647	PPM-97-029
19	AD562	12 bit DAC	24 Pin DIP	AD/PMI	2.5-125	35	50	8742	PPM-97-029
20	29AMDF016	16MB EEPROM,5V	48 Pin TSOP	AMD	5-15	10	10	Not Marked	PPM-97-011
21	AS58C1001SF	Rad-Hard EEPROM	32 Pin FP	ASI	5-100	30	>100	9646	PPM-97-034
22	SD5000B	DMOS	TO-8	CAL-Logic	2.5-50	2.5	6	93-2629W#1	PPM-97-046
23	SD500A	DMOS	16 Pin DIP	CAL-Logic	2.5-50	5	7.5	93-2629W#1	PPM-97-045
24	SD5000	Power MOSFET	16 Pin FP	CAL-Logic	2.5-7.5	5	7.5	9633	PPM-97-009

Table 1: Low Dose Rate TID Test Results for Parts Tested in 1997 /1 /2 (Continued)

S/N	Generic Part No.	Part Type	Package Type	Mfr.	Test Level, krads(Si)	Init. Deg Level, /3 krads(Si)	Sig. Deg Level, /4 krads(Si)	LDC /5	Report
25	2N6849	Transistor	TO-39	Harris	5-50	10	20	9646	PPM-97-040
26	2N6796	Transistor	TO-39	Harris	5-50	5	20	9637	PPM-97-039
27	MHV2803R3	DC/DC Converter	10 Pin Hermetic	Interpoint	5-100	5	10	9712	PPM-97-037
28	LT1009	Voltage Reference	TO-18	Linear Tech.	2.5-100	30	100	9543	PPM-97-027
29	LM137	Voltage Regulator	TO-39	Linear Tech.	2.5-50	10	15	9638	PPM-97-020
30	MX7847	D/A Converter	24 Pin DIP	Maxim	2.5-100	20	30	9707	PPM-97-025
31	4429	MOSFET Driver	8 Pin DIP	Micrel	5-100	5	30	9309	PPM-97-058
32	LM137	OP AMP	TO-39	National	10-200	30	100	9328	PPM-97-043
33	LM117HV	OP AMP	TO-39	National	10-200	20	200	9054	PPM-97-042
34	LM117H	OP AMP	TO-39	National	10-200	50	>200	9305	PPM-97-041
35	54ACT245	Transceiver	20 Pin FP	National	5-100	50	100	9637	PPM-97-052
36	LM317AT	Voltage Regulator	TO-220	National	5-100	20	30	M73BL	PPM-97-051
37	LM105	Voltage Regulator	TO-5	National	5-100	>100	>100	9640	PPM-97-033
38	LM137	Voltage Regulator	TO-39	National	5.0-100	10	30	9615	PPM-97-030
39	54ACT245	Transceiver	20 Pin DIP	Phillips	5-100	20	30	9722	PPM-97-054
40	OP07	OP AMP	20 Pin LCC	PMI	5-100	10	20	9446	PPM-97-038
41	KM48C,V8100AS-6	4Mx8 DRAM	32 Pin SOIC	Samsung	2.5-100	10	30	Not Marked	PPM-97-017
42	W48C20	PEM Clock	8 Pin SOIC	Samtec	2.5-150	>150	>150	Not Marked	PPM-97-026
43	SHD3166	Diode	SHD1	Sensitron	5-100	>100	>100	9706	PPM-97-047
44	UC1707	PWM	20 Pin LCC	Sensitron	2.5-100	>100	>100	9649	PPM-97-048
45	JANTXV2N6661	Power MOSFET	TO-5	Siliconix	2.5-30	15	20	9636	PPM-97-010
46	2N2880	Transistor	TO-5	Solitron	2.5-100	>100	>100	9644	PPM-97-049
47	TMS416400	16 Mbit DRAMS, 5V	24 Pin SOJ	TI	5-12.5	10	12.5	Not Marked	PPM-97-006
48	TL7770-5	Power Supervisor	20 Pin LCC	TI	2.5-50	2.5	30	9537	PPM-97-044
49	TL7705	Power Supervisor	20 Pin LCC	TI	2.5-30	15	30	9543	PPM-97-014
50	54ACT245	Transceiver	20 Pin DIP	TI	5-100	15	30	9717	PPM-97-053
51	UC1706	PWM	20 Pin LCC	Unitrode	2.5-100	>100	>100	9533	PPM-97-055

Notes:

1. The information was developed for general guidance only under GSFC laboratory test conditions (as detailed in PPM reports). These conditions may differ substantially from outside lab conditions.
2. The information should not be construed as a representation of product performance by either GSFC or the manufacturer.
3. The initial degradation level is the radiation exposure level where the parts first deviated from the manufacturer's pre-irradiation specification limits.
4. When the parts performance degrades with TID exposure, the determination of whether the degradation is significant or not, varies with the application of the part in the circuit. It is therefore difficult to define a single significant degradation level for each part type. The significant degradation level provided here is based on our judgement of the parts performance and circuit application. This level may be higher or lower for different applications. **Designers should review the individual part report before making a decision on the suitability of the part from a TID aspect, particularly if the design has a very narrow tolerance from the specification limits for any electrical parameter.**
5. The radiation exposure response of these commercial parts can vary significantly with LDC due to any process and / or design changes by the manufacturer.

Defects, in "PPM" Parts of What? Per Million of What? and Why?

Tom Clifford
Process Specialist
Lockheed Martin Missiles and Space
(408) 742-6950
tom.clifford@1mco.com

Several years ago, we entered the world of ppms (defects, in parts per million). Process engineers knew that systematic tracking of defects could guide cost-reduction efforts. Marketeers would sell their assembly capability by touting a certain Cpk or sigma quality level. Procurement managers needed an easy way to select contract assemblers. Plant management wanted a measure of operations performance. The ppm quality metric became the name of the game. However, this metric has not yet been universally implemented or accepted. After optimistic kick-offs, systems were abandoned or dwindled in importance. The effort seemed excessive, compared to the value of the defect counts.

Why was this happening? Perhaps, the ppm numbers weren't as unambiguous a measure of quality as everybody had hoped. This deceptively simple measure masks some powerful hidden assumptions that can lead to significant misunderstandings and distortions.

Why should there be any misunderstanding? The concept is simple:

A "defect" is straightforward. Well-crafted workmanship standards exist (e.g. J-STD -001, MIL-STD-2000, NHB-5300.4, and IPC-A-610, for instance) that describe defective solder joints and other defects.

There are good tools available to detect defects and to accumulate defect numbers.

The calculation is simple: "ppm" is simply the number of defects per million opportunities.

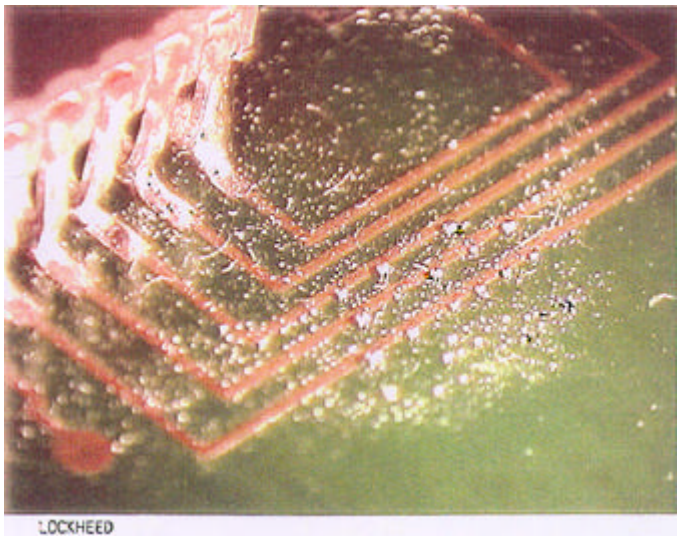
What could be easier? ..... However:

Is a misregistered 144 I/0 QFP one defect, or one hundred forty-four bridges, opens and off-the-land defects?

Is a spray of solder balls one defect or is it several hundred? How about an assembly with several isolated white stains..? One defect or many?

When a potential supplier brags about 3 ppm, is he saying that he really looked at millions of joints and found only three bad ones per million? Before touch-up? That's good. However, if it's three field failures per million joints shipped, that's bad.

How do you compare one shop that includes minor defects, process indicators, and cosmetic blemishes in their ppm count vs another shop that counts only functional failures?



Solder Balls - one defect or several hundred?

- How do you describe a QFP with one bent-down lead: Is it many opens? Is it only one damaged lead? Do you count the one cause or the many symptoms?

Each of us is convinced that his understanding of "ppm" is correct , but each of us has a different perspective and a different objective, all perfectly valid. Experienced workers will disagree, honorably. This paper discusses some problems in the definition, calculation, and application of the ppm metric, as well as some consideration of root causes. Its intent is to provide visibility; not to resolve the issues. That resolution will take consensus inside each company, guidelines within the industry, and communication between supplier and customer.

The examples reflect SMT experience, but the concepts apply equally to any assembly operation. This paper does not discuss definitions of defects, inspection tools, training, SPC, or data management software. These are well covered elsewhere. Those

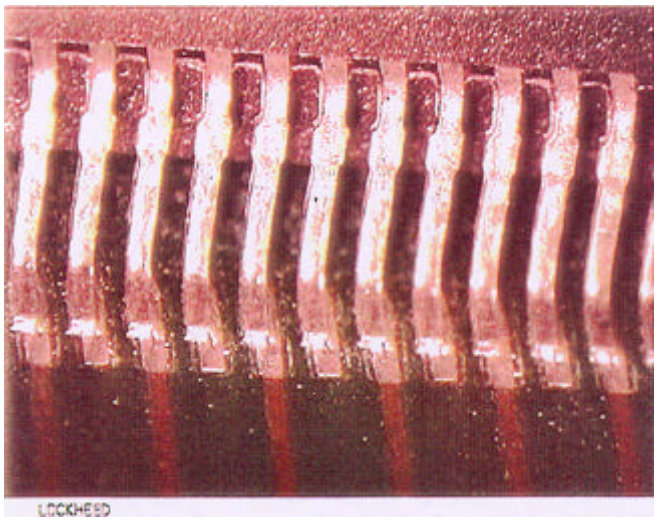
tools and skills are important, but they all depend on and implement the concepts and decisions discussed herein.

If your system truly intends to calculate ppms, or DPMO (defects per million opportunities), certain concepts must be resolved up-front. First, decide what **categories of defects** are to be included. Do you include everything: process indicators, cosmetic blemishes, minor, major or critical defects, and test or field failures? There will be far more cosmetic defects than there will be test failures. If you have a strict "continuous improvement" discipline in place, you'll have Pareto analyses sending you off to fix cosmetic attributes, while the few functional defects get lost in the noise. Focus primarily on tracking the major, critical, functional defects. Process indicators and cosmetic defects could then be included in a less rigorous format. Don't blindly clump the categories together. Note that it costs a lot of money to capture and manage defect data; so your resources should be directed towards the most influential defect data.

Next, decide how to handle **externally-caused defects**, such as defective components or troublesome designs. Including them will guide enterprise-wide improvement efforts. Correcting them will dramatically improve shop performance. However, if your objective is only to track internal operations performance, then these external causes must be excluded, and then handled separately.

Then, the fundamental issue of **count definitions** must be resolved. As suggested earlier, several types of defect can be troublesome.

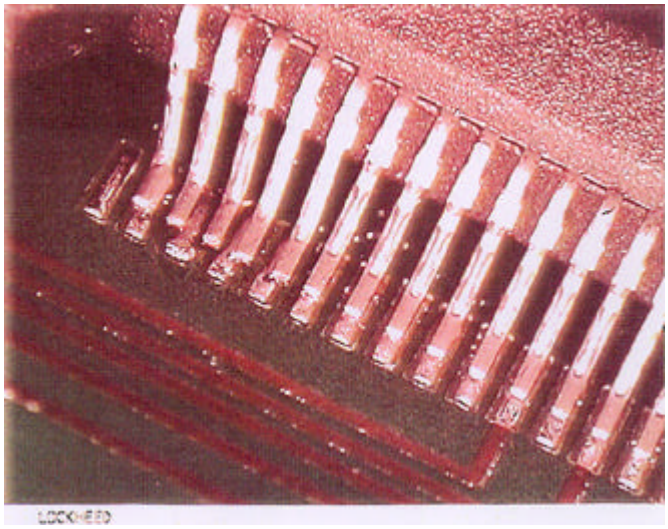
- Misregistration. A lead too far over the edge of the land is a defect. Misregistration during placement, or a shift before or during reflow typically causes most of the leads to be off the land and therefore defective. Should the count be one (misregistered component) or many (individual leads)? The latter case would be a very large defect count, resulting in a very high ppm value. This could incorrectly skew the data.



Misregistration -- How many defects?

Another option is to count the number of edges that are off. Often only two edges are affected (caused by a simple X or Y translation). If the QFP is shifted in both X and Y or is twisted, all four edges could have leads off their lands. This feels like a defensible approach: it weights the data fairly and discriminates among severities of misregistration.

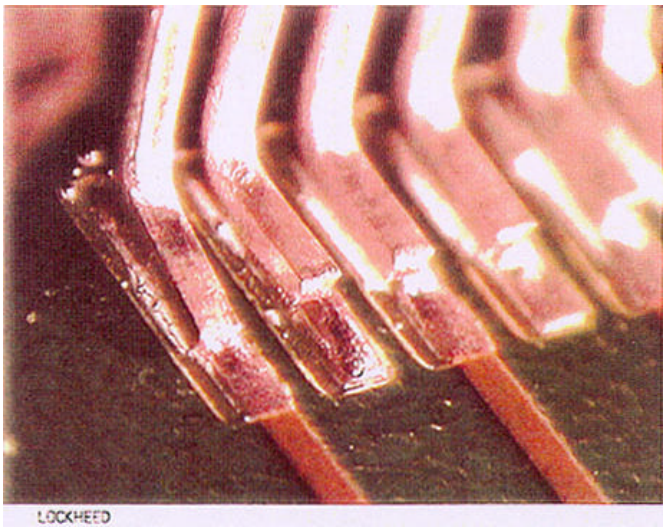
- Bridging. An isolated bridge is typically a symptom of solder-paste mis-print, a mis-positioned component, or a damaged lead. Often, gross bridging is associated with many solder-balls, opens, and excess or insufficient solder, and is the symptom of a specific cause. Should the count be one, to suggest one cause for the situation, or should it be many, to reflect the many symptoms?



One "sweep"?, or several bridges and off-lands?

For gross bridging, a good idea is to count the number of edges at which the condition appears. If bridging is associated with damage (swept or splayed QFP leads, for instance), the count should reflect the number of damage events, not the number of affected leads.

- Opens Usually an open is a symptom of a damaged lead, a mis-print or mis-position, or a non-wetting condition. An isolated open should be counted individually. However, a series of opens, along one or more edges of a flat-pack, that are obviously related to a specific cause (such as damage or non-wetting), should be counted as one defect.

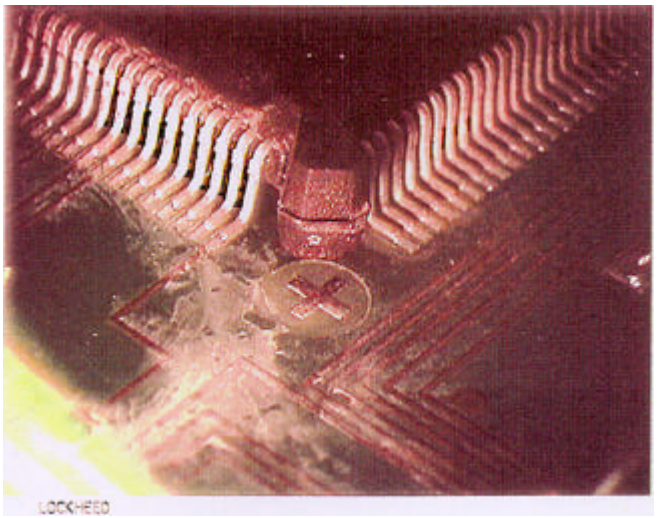


One "toe-down damage"? or many "opens" + "insuf fillets" ?

- Solder-balls. One defect or several hundred? A preferred approach is to count the number of components near which the condition appears. This offers a proper balance, and is consistent with root causes which can operate at a local, component, level.

- Non-wet. A blotchy non--solderable condition can affect components leads as well as the PWB lands. Is this to be counted as many solder fillet defects? or one defective PWB? or one or many bad components?

- Contamination and stains. This is a similar situation. A count of one stained assembly would underreport the events; a count of all the many local stains or contaminant points would be impossible to do, and could over-report the event. Again, the best compromise might be to count the number of components that are associated with the contamination. Note that several different types of contaminants would trigger several additional counts.



Contamination ... one count ?

The list could go on. One cause or many symptoms? The count as well as the code must be established. Decisions should be documented, to cover most of the anticipated conditions. These positions need to be thoroughly conveyed to the operation and inspecting staff, to ensure that the correct defect counts get reported. A trial period, to work out the bugs, then some fine-tuning, makes sense.

These decisions, and the ones below, will have a dramatic effect on the absolute level of reported ppm values. Make the selection to optimize the information value, not to get the lowest ppm values. Also, don't change the defect-count rules in mid-stream. That will trigger dramatic changes in apparent performance, and should be minimized and done with visibility.

How do we establish the **number of opportunities**? The divisor, the number of opportunities, must be well-considered and explicitly stated. The rationale for defining this number must be linked to the intended defect-counting scheme. The math must suit the task. Select one: the number of assemblies? the number of components? the number of solder joints? joints plus components? There is even statistical justification for totaling the number of opportunities

for each defect to happen, which would result in a very large opportunities number: several times the number of solder joints. There are good reasons and applications for any of these choices. MIL-STD-2000 offers some guidance in this regard, in its "normalizing" number.

Take one example: if you intend to monitor defective incoming components, the math would be simple: "opportunities" would be the total number of components inspected; and the "number of defects" would be the number of bad components. If you intend to monitor final test, the defects would be fails and the opportunities would be the number of assemblies. However, typical SMT assemblies are much more complex. There can be several independent defects on the same solder joint. There can be defects that are directly linked only to the component. There also can be defects associated with no particular component at all. Thus, there are opportunities related to solder joints as well as opportunities associated with components, and opportunities associated with the assembly itself.

One approach is simply to count the solder joints, as the number of opportunities. This under-represents the number of opportunities not related to the solder joints. As suggested above, an extreme scheme would multiply the number of joints by the number of defects that could possibly affect each joint. This would result in a huge divisor and would result in low ppm values. A preferred mid-range approach is to define the number of opportunities as the number of joints plus the number of components. This compromise is an attempt at a fair count of joint-related and component-related defects, plus it can be readily calculated. It is favored in MIL-STD-2000.

A hypothetical example case, to show the impact of some of these uncertainties, might look something like this: Assume a days production of two hundred 2-sided SMT assemblies. Each assembly has two 296 I/O QFPs, two 144 I/O QFPs, eight 28 I/O FPs, twelve 14 I/Os FPs, twenty-four SOTs, and 36 passives. Assume that 100% verification of that day's production revealed the following defects: one big QFP seriously misregistered resulting in all leads off-the-land, plus ~five assorted opens and bridges; two mis-registered 28 I/O FPs; and a spray of solder-balls (~ 50 solder-balls) behind one of the QFPs on half of the assemblies. Assume further that only the opens and bridges would cause test failures. What is the defect level, in ppm?

Case 1 The number of opportunities is set to be equal to the number of solder joints. Each defective item is counted. **16238 ppm**

Case 2 The number of opportunities is the number of solder joints plus the number of components. The collective defects are counted as the number of components affected, other defects are all counted individually. **153 ppm**

Case 3 The number of opportunities equals the number of solder joints plus components. Only the test failures are counted as defects. **15 ppm**

Did you really look at all the opportunities? If you intend to talk about ppms, 100% inspection is required. You cannot calculate ppms, legitimately, unless you actually look at each one of the opportunities. Conversely, a scheme that simply spot-checks some of the most typically troublesome features (which is often the case) cannot properly assert that it is truly 100% inspection, and therefore cannot rigorously report results in ppm. Some alternate schemes are based on operators looking at specific features of the assembly at several places along the process. It can be argued that this probably accumulates enough verification to justify an assertion of 100% inspection. This argument will feel right to a conscientious process operator, but would not convince a statistician. Check around, and get buy-in, before you get too far along with that approach.

In summary: Reported ppm values must always be received skeptically. Typically, good data is lurking there, but that needs to be explored. Understand the "defect" and "opportunities" definitions. Check for trends over time, and check that the categories and definition aren't changing. Require a written description of the mathematical bases. Work with your customers and your management to define exactly what is expected of the quality system. Systems tailored for bench-marking or for marketing will be structured differently than systems intended to optimize process performance. The math (defect counts and opportunities) as well as the scope (level

of defects, external causes, rework, etc.) should be tailored to the task, but must be internally consistent.

ACKNOWLEDGMENTS

The author acknowledges the support of the SMT crew at Lockheed Martin Missiles & Space, Sunnyvale; particularly Yun Wang, Manufacturing Engineer, Paul Smick, Procurement Manager, and Dwayne Komush, Design Consultant.

Low Temperature Power Electronics Program

Richard L. Patterson
NASA Lewis Research Center
(216) 433-8166
Richard.L.Patterson@lerc.nasa.gov

John E. Dickman
NASA Lewis Research Center
(216) 433-6150
John.E.Dickman@lerc.nasa.gov

Ahmad Hammoud
NYMA, Inc
NASA Lewis Research Center
(216) 433-8511
Ahmad.hammoud@lerc.nasa.gov

Scott Gerber
NYMA, Inc.
NASA Lewis Research Center
(216) 433=8059
Scott.S.Gerber@lerc.nasa.gov

INTRODUCTION

Many space and some terrestrial applications would benefit from the availability of low temperature electronics. Exploration missions to the outer planets, Earth-orbiting and deep-space probes, and communications satellites are examples of space applications which operate in low-temperature environments. Space probes deployed near Pluto must operate in temperatures as low as -229°C.[1] Figure 1 depicts the average temperature of a space probe warmed by the sun for various locations throughout the solar system. Terrestrial applications where components and systems must operate in low-temperature environments include cryogenic instrumentation, super conducting magnetic energy storage, magnetic levitation transportation system, and arctic exploration. The development of electrical power systems capable of extremely low-temperature operation represents a key element of some advanced space power systems.

The Low-Temperature Power Electronics Program at NASA Lewis Research Center focuses on the design, fabrication, and characterization of low-temperature power systems and the development of supporting technologies for low-temperature operations such as dielectric and insulating materials, power components, optoelectronic components, and packaging and integration of devices, components, and systems.

PROGRAM

The goal of the low-temperature program is to develop and demonstrate reliable, efficient, power systems capable of surviving and exploiting the advantages of low-temperature environments. The targeted systems are mission-driven and include converters, inverters, controls, digital circuits, and special-purpose circuits. Initial development efforts have produced the successful demonstration of low-temperature operation and cold-restart of several DC/DC converters (with outputs from 5 to 1000 Watts) utilizing different design topologies.[3-5] Some of these circuits employed superconducting inductors.

In support of system development, device and component research and development efforts are underway in critical areas of passive and active components, optoelectronic devices, and energy generation and storage. Initially, commercial devices and components are being characterized at low-temperatures. Where there does not exist a viable commercial device or component, a development effort is undertaken.

In addition to the development efforts to fill the key holes in low-temperature power electronics, thermal issues relating to packaging, integration, and cycling are being explored.

LOW-TEMPERATURE DEVELOPMENTAL FACILITIES

At NASA Lewis Research Center, facilities exist for the testing of power and control circuits operating from DC to several Megahertz over a wide temperature range. These facilities consist of a liquid nitrogen cooled environmental chamber in which a circuit can be operated with controlled temperature in the range of 300°C to -185°C. Measurement and test equipment include a digital signal analyzer, precision digital multimeters, precision temperature controller and recorder, 3kW electronic load, and resistive loads from mW's to kW's in power.

A complete computer-controlled semiconductor device characterization system is used in conjunction with a cryopumped vacuum chamber containing a cryocooled sample holder to characterize commercial

and developmental devices and components. This facility is capable of in-situ current-voltage (I-V) and capacitance-voltage (C-V) characterization of semiconductor devices from 23°C to -248°C.

Lewis has built computer-controlled facilities for low-temperature thermal cycling and characterization of electrical and physical properties of dielectrics and capacitors. In addition, facilities have been built at Lewis for reliability studies and life testing of capacitors and other components in space-like environments under multi-stress conditions.

In the area of optoelectronics, Lewis has facilities to characterize and test fiber-optic sources, receivers, cables, connectors, and other components and assemblies at temperatures from 300°C to -185°C. Although most low temperature testing on fiber-optic components has concentrated on 1300 nm to date, tests can be conducted at other wavelengths.

CONCLUSION

The Low-Temperature Power Electronics Program at NASA Lewis Research Center is developing selected, mission-driven, power systems and supporting technologies for low-temperature operation. Coordination of these and other related research and development efforts are always encouraged and are implemented with other U.S. Government agencies, academia, and the aerospace industry.

REFERENCES

1. B. Ray and R. Patterson, "Wide Temperature Operation of a PWM DC-DC Converter", IEE Industry Applications Society Conference, Orlando, FL, October, 1995.
2. Private Communication with Jeff George, NASA Lewis Research Center, August, 1994.
3. B. Ray, S. Gerber and R. Patterson, "Liquid Nitrogen Temperature Operation of a Switching Power Converter", Low Temperature Electronics and High Temperature Superconducting Symposium, Reno, NV, May, 1995.
4. B. Ray, S. Gerber, R. Patterson, "Low Temperature Performance of a Full-Bridge DC-DC Converter" IECEC 96, Vol. 1, Washington, D.C. August, 1996.
5. B. Ray, S. Gerber, R. Patterson, and J. Dickman, "Low Temperature Performance of a Boost Converter with MPP and HTS Inductors," IEEE APEC 96 Conference, Vol. 2, 1996.

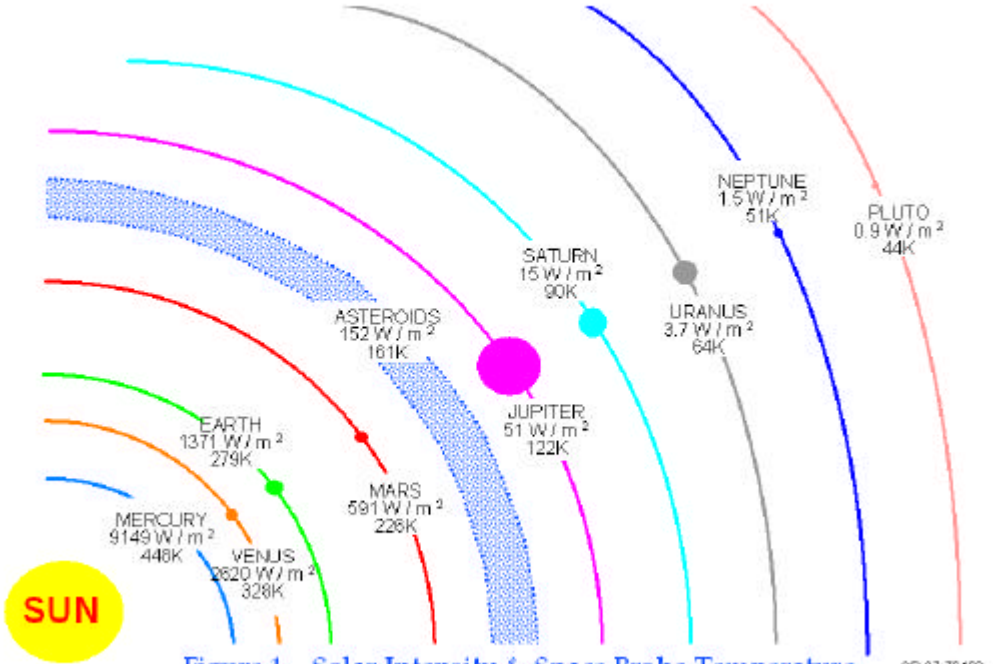


Figure 1. Solar Intensity & Space Probe Temperature

High-Speed Thermal Cycle Life Test of Thin Film Specimens

Charles E. Powers
NASA Goddard Space Flight Center
Code 313
(301) 286-8061
cpowers@pop300.gsfc.nasa.gov

In support of the Hubble Space Telescope (HST) Multilayer Insulator (MLI) Failure Review Board, the Materials Engineering Branch (MEB) was requested to perform a high-speed thermal cycle life test of candidate materials to be used to replace the existing HST thermal blankets during the next servicing mission. As part of the environmental test of the candidate replacement materials, the test samples needed to be thermal cycled 20,000 to 70,000 times between +50°C and -100°C. The test samples were typically 1 x 3 inches and were between 5 and 10 mils thick. To accomplish this testing in a reasonable amount of time, the MEB developed a setup using liquid nitrogen and a hot air gun that is capable of completing a cycle in 15 seconds.

Liquid nitrogen (LN2) and a hot air gun are used to thermal cycle the samples (see Figure 1). The samples are cooled to below -100°C by flowing LN2 (as well as gaseous nitrogen) over the samples. A phase separator is attached to the end of the LN2 inlet to produce a more even flow of LN2 over the samples. The samples are then heated by use of a hot air gun. In this particular case the hot air gun flows gaseous nitrogen (N2) over the samples, because the entire setup is located inside a N2 purged thermal chamber. This chamber is under constant N2 purge to prevent moisture from condensing or freezing on the samples.

A solid state relay (SSR) is used to open and close a valve that controls the flow of LN2. Another SSR is also used to turn the hot air gun on and off. A square wave generator is used to toggle the SSRs. When the signal from the generator is one volt, the SSR controlling the LN2 opens the valve and the SSR controlling the hot air gun is turned off. When the signal from the generator is zero volts, the SSR controlling the LN2 closes the valve and the SSR controlling the hot air gun is turned on. The signal from the generator is conditioned through a couple of amplifiers (one for each SSR) before reaching the SSRs.

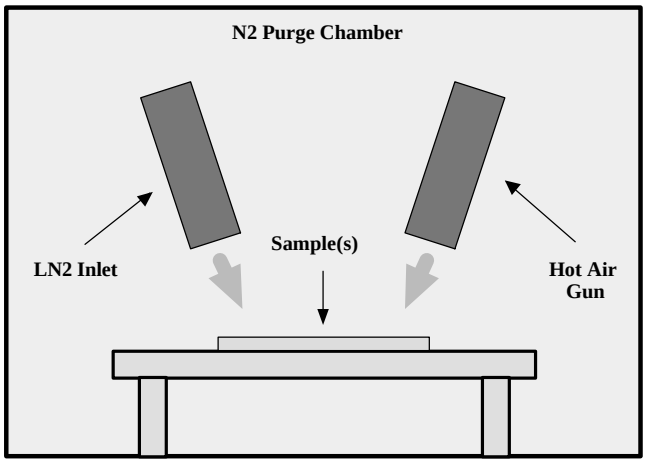


Figure 1. Schematic diagram of high-speed thermal cycling setup.

The duty cycle of the square wave is adjusted to achieve the desired thermal cycle. For most of this testing, the LN2 valve was opened about 38 percent of a cycle and the hot air gun was on for the remaining 62 percent of the cycle. Several thermocouples were mounted to the test fixture holding the samples and directly to a control sample to monitor temperature and to adjust the duty cycle of the square wave. The samples were taped and clamped to the test fixture as shown in Figure 2.

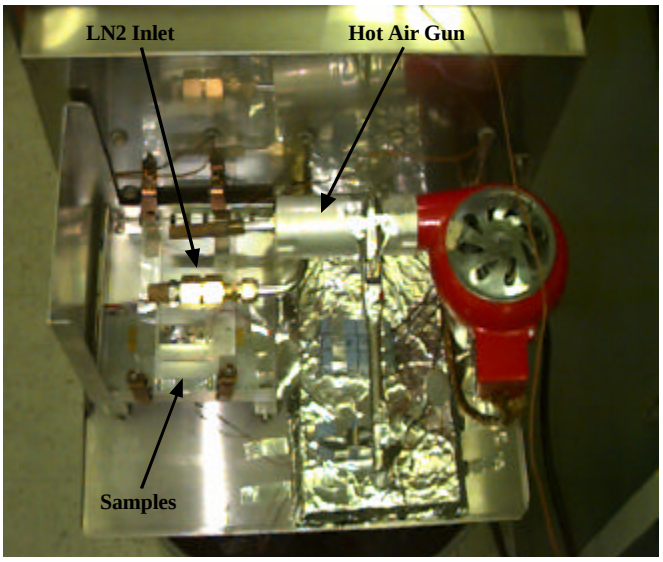


Figure 2. Photograph of high-speed thermal cycling setup.

The author would like to thank Bruno Munoz (313/Unisys) for his work in developing this test setup. Mr. Munoz constructed the entire setup and was instrumental in its design.

Mr. Charles E. Powers is an electronics engineer in the Materials Engineering Branch at NASA Goddard. He has been developing specialized experiments since 1983. He also serves as the materials assurance engineer for Goddard spacecraft. He has an M.S. in Physics from the American University.

Mr. Bruno Munoz is a technician in the Materials Engineering Branch at NASA Goddard. He has also been involved in developing specialized experiments while working in the Materials Engineering Branch. Bruno has been working at Goddard through Unisys for 14 years and has an A.A. in Electrical Engineering Technology from Montgomery College.

First Annual Microelectromechanical System (MEMS) Reliability and Qualification Workshop

Steve Bolin
Jet Propulsion Laboratory
818-354-3699
steve.bolin@jpl.nasa.gov

The first Microelectromechanical System (MEMS) Reliability and Qualification Workshop was held at the Jet Propulsion Laboratory on August 5, 1997. The workshop was sponsored by the JPL Office of Engineering and Mission Assurance and the NASA Office of Safety and Mission Assurance. The following presentations were made:

MEMS Issues For Human Mars Exploration
Dr. Andrew Benjamin; NASA-Johnson Space Center

Radiation Issues For MEMS Devices
Dr. Charles Barnes; JPL

Wafer Production Issues For The MEMS Industry
Michael McEntee; Standard Microsystems Corporation

Process Qualification For Fabrication Of Advanced MEMS Devices
Dr. Chris Constantine; Plasma-Therm Incorporated

The Role Of Damping Gas On Ribbon Impulse Response
Chris Gudeman; Silicon Light Machines

Tribological Behavior of Polycrystalline Diamond & Poly-Single-Crystal Silicon in Vacuum and Hydrogen For MEMS Micromechanical Applications
Michael Gardos; Hughes Aircraft Company

Fatigue Crack Initiation and Growth Testing Of MEMS and "Small" Structures
Christopher Muhlstein; Failure Analysis Associates

MEMS Activities at JPL
Bill Tang, JPL

Quality and Reliability Assurance Of Microelectromechanical Devices
Paul Ratazzi and George Ramseyer; Rome Laboratory /ERDA

Methodology For MEMS Reliability Evaluation and Qualification
Sammy Kayali; JPL

A Physics-Of-Failure Based MEMS Qualification Methodology and It's Application To The Vaporizing Liquid Microthruster
Andrew Wallace, Kin Man, and Juergen Mueller; JPL

Reliability and Failure Analysis Of MEMS At Sandia National Laboratories
W. Eaton, D. Tanner, N. Smith, D. Bowman, and K. Peterson; Sandia National Laboratories

Use Of NDE For Quality Improvement of MEMS
Steve Bolin and John Olivas; JPL

Presentations are available at:
http://eis.jpl.nasa.gov/quality/qa/Aip/mwrkshop/toc.html

To be placed on the mailing list for future meetings, please contact Steve Bolin, Sammy Kayali, or Kin Man at the Jet Propulsion Laboratory.

Programmable Logic Application Notes

Richard Katz
Microelectronics and Signal Processing Branch
Goddard Space Flight Center
301-286-9705
rich.katz@gsfc.nasa.gov

This column will be provided each quarter as a source for reliability, radiation results, NASA capabilities, and other information on programmable logic devices and related applications. This issue includes some design application notes and some recent radiation test results of interest.

NEW WWW SITE FOR PROGRAMMABLE LOGIC AND DEVICES

A new WWW site dedicated to the design and use of programmable and quick-turn technologies for space flight applications (http://rk.gsfc.nasa.gov) is available. This site is intended to complement this column. As such, the EEE Links columns will be shorter with more information (with a higher level of detail) available on-line. The site is still a bit new and more information is constantly being added with older reports and papers being put on line and new results rapidly being posted.

The site will cover several categories of programmable devices such as FPGAs, PALs, memories such as EEPROMs, and programmable substrates. For each topic area, there are three sub-areas: design application notes, radiation test results, and links to manufacturers sites for access to commercially available information. Two pages are dedicated to technical papers and presentations concerning programmables - typically radiation or reliability information. Other pages include useful information such as links to socket manufacturers, sites with radiation information, general design information, and industry links. Comments and submissions are always welcome.

CHIP EXPRESS UPDATE

Two rounds of heavy ion tests have been completed on our CX2041 LPGA prototypes. The first round was conducted at V_{CC} = 5.0 volts and these epi-based devices readily latched. Further testing was performed at VCC = 3.3 volts and the samples latched quickly with Bromine (LET = 37 MeV-cm^2/mg). The CX2041 model has embedded SRAM. The CX2030, which does not have SRAM, is planned for testing in February 1998.

As discussed in the last edition, we were building an in-flight radiation experiment. This has been delivered (see notes below) and included QYH530 and CX2041 packaged both in MQFP208's and on a Pico Systems antifuse programmable substrate/MCM.

RADECS '97 PAPER

"Antifuse FPGA for Space Applications" has been accepted for RADECS '97. *Abstract*: This paper presents total dose and SEE testing data of recent antifuse products. It includes ONO-antifuse FPGAs: A1020B, A1020S, RH1020, A1280XL, A1460A, A14100A, A32140DX and A32200DX. Also included are preliminary results of pre-production metal to metal (M/M) antifuse FPGAs, the I100 and the RHI100. Finally, SEU rate calculations of Actel FPGAs are discussed.
http://rk.gsfc.nasa.gov/richcontent/fpga_content/rad97_v3.pdf

RECENT TEST RESULTS ON PALS: CYPRESS BICMOS 22V10C DEVICES

Here's a summary of some recent heavy ion and proton tests of PALs.
www link: http://rk.gsfc.nasa.gov/richcontent/pals/Cypress22v10Sep-97.PDF

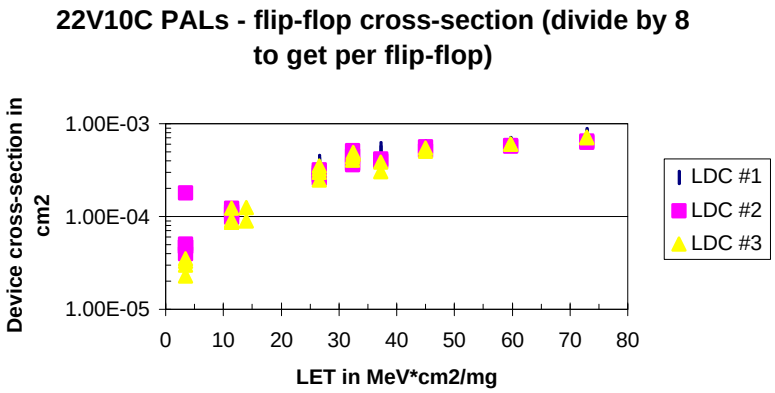
Test mode: Dynamic, 1 MHz, shift register of alternating 1's and 0's

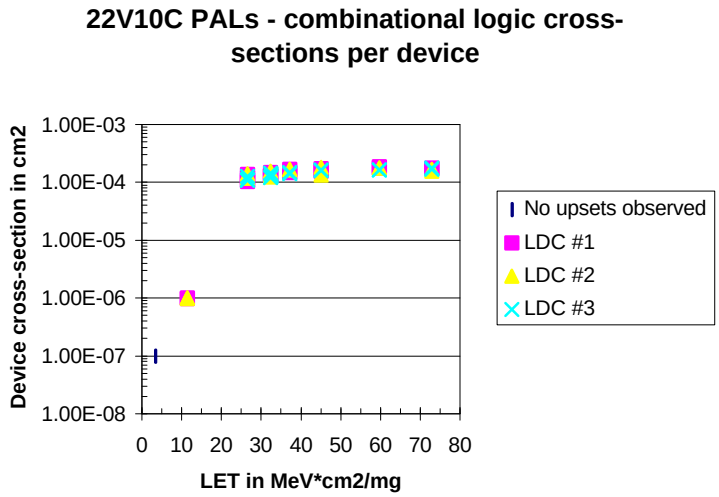
Protons at UCD (6/97)
Mfr: Elmo (Cypress die)
Part #: JT22V10-10 ETUFP (Jackson and Tull part number)

Results: Upsets in flip-flops with 63 MeV protons.

Cross-section is 2E-11 per flip-flop
No upsets in combinational logic gates

Heavy ion tests at BNL (7/97)
Results for 3 LDCs are graphed below.
LDC #1 002611202
LDC #2 XC34950484
LDC #3 XC349608493





DETECTING ASYNCHRONOUS LOOPS WITH DESIGNER

Abstract: Current versions of Designer timing analysis software do not automatically notify the analyst of asynchronous feedback loops in their design. These warning were the default for earlier versions such as ALS 2.3.2. This checking can be done as described below.

To make DTAnalyze issue a warning if it senses an asynchronous loop perform the following operation. Under the Options menu, use the Set command to set the variable "showbreakloop" to "1" (without the quotation marks). The Set command setting can be verified by using the Get command, also under the Options menu, which will print the "showbreakloop" variable's value in the main status window. Now, when a timing analysis is performed, a warning should appear in the main status window indicating any asynchronous loops and which pins were put into a break set.

Here's sample output from a simple design using cross-coupled NAND gates to make an RS flip-flop.

> *Variable showbreakloop = 1;*
> *Pins 'G2:A' has been put into STOP set to break loop.*

USING SYNOPSIS TO DESIGN FLIP-FLOPS FOR THE RADIATION ENVIRONMENT

Abstract: This application note shows how to use Synopsis automation scripts to control synthesis such that SEU soft flip-flops (S-Module flip-flops) are excluded from the synthesized output. The synthesis can be controlled to either use radiation-tolerant flip-flops (C-Module or C-C flip-flops) or triple-modular redundant (TMR) structures. For the full application note, see http://rk.gsfc.nasa.gov/richcontent/fpga_content/synopsis_actel.pdf.

ACT 3 TECHNOLOGY AT 125 MHz

Abstract: Simulations were run on a simple circuit to determine the feasibility of running Actel Act 3 devices at 125 MHz (8 nSec cycle time) with two levels of logic between flip-flops and high-slew output buffers being used. The simulations determined chip-to-chip timing as well as internal timing and were run over a variety of models, speed grades, and environmental conditions.

EVALUATION OF 125 MHz CIRCUITS IN ACT 3 FPGAS

Simulations were run on a simple circuit to determine the feasibility of running Actel Act 3 devices at 125 MHz (8 nSec cycle time) with two levels of logic between flip-flops and high-slew output buffers being used. The simulations determined chip-to-chip timing as well as internal timing and were run over a variety of models, speed grades, and environmental conditions.

Here are the results:

Device	Speed	Cond	t_{SU}	t_H	REG REG	CLK PAD
A1425A	-1	MIL	2.9	-1.0	10.4	10.4
A1425A	-2	MIL	2.9	-1.4	9.1	8.7
A1425A	-2	COM	2.6	-1.2	7.9	7.5
A1425A	-3	MIL	1.8	-0.3	8.2	8.7
A1425A	-3	COM	1.5	-0.3	7.1	7.5
A1460A	-1	MIL	3.3	0.4	10.9	11.7
A1460B	-1	MIL	2.5	1.6	10.1	11.7
A1460BP	-1	MIL	2.5	1.6	10.1	11.7

An attempt was made to place and route the A1425A-2, with military derating, using timing-driven place and route with a constraint of an 8 nSec clock period. The attempt failed with a negative slack of -1.2 nSec.

CONCLUSIONS AND NOTES

1. There are timing differences between the A1425A and the A1460A, with the A1425A being faster in several categories, with about a 5% improvement in register-to-register performance.

2. 125 MHz operation does not appear feasible in this configuration with two logic levels between flip-flops.

3. The 'B' series devices have a very significant positive hold time.

4. Getting data on-chip at high speeds seems feasible. Note, however, that the SEU-soft I/O-Module flip-flops must be used.

5. Getting the data off-chip is also a critical path and will limit system performance.

PGA TO QFP WORK-A-ROUND FOR DESIGNER

A problem was encountered with Designer 3.1.1 when repackaging an A14100A PGA257 design to a CQFP256 design. Actel has stated that this will be fixed in the next revision of software and has quickly provided the following work-a-round. This bug did not show up in Designer 3.0 and it appears to be limited to versions 3.1 through 3.1.1U1.

The bug is that the software doesn't save any "compatible" die or package changes in the database. If you changed to a package or die that forced you to re-layout the design, then the information gets saved properly. The problem only occurs if you change to a package or die that doesn't require a re-layout, a compatible die change. This feature is used, for example, if a prototype is done in a PGA package and a flight QFP device needs to be programmed - obviously, no die changes eliminates the need to rerun the timing analysis and possibly modify the design or place and route. This is a general software bug, not related to the type of device being used.

The procedure is to manually set the "package" variable, then re-generate the AFM file. To do this:

1. First, verify which package is currently selected. In Designer, go to the top level Options menu and select Get. Under "Variable:", type in "package" (without the quotes), then select OK. In the status window below, you will see either

   Variable package = pga257 (if the 257 pin CPGA package was selected) or Variable package = qfp256 (if the 256 pin CQFP package was selected)

2. To set the package type manually, in the Options menu, select Set. Under "Variable:", type in

"package" (without the quotes). Under "Value:" type in either pga257 or qfp256, depending upon which one you want, then select OK.

3. After changing the package, nothing will happen. The display at the bottom of the screen will still show the old package, but if you use the Get command as in step 1) above, the value of the variable "package" should show the new value. Always verify that the variable "package" was set properly, as we don't check the variable values very carefully when they are entered manually.

4. Re-generate the AFM file by clicking on the Fuse button. You can verify that none of the fuses changed by "diffing" the old and new AFM files. Only one line should be different and that is the line that contains the package type. If you are VERY, VERY careful, you can edit the AFM file directly to change the package type, but I am reluctant to recommend this, as it is so easy to make mistakes when manually editing files.

METASTABLE STATES

INTRODUCTION

Normally a flip-flop is one of two states; either storing a logical '1' or a '0'. These states are stable as flip-flop elements employ positive feedback. In properly designed and functioning systems, all flip-flop parameters are met and the device operates normally. The key parameters are setup time, hold time, and pulse width (for clocks, presets, clears, jam loads, etc.). If these parameters are violated, as when an asynchronous input is fed into a flip-flop without meeting the setup and hold times, or when a runt pulse is input into the clock or asynchronous preset/clears, the flip-flop may go "metastable."

Device behavior in the metastable state may manifest itself as increased CLK -> Q delay, device output being a non-logic level, or an output switching and then returning to it's original state. Theoretically, the amount of time a device stays in the metastable state may be infinite; in practical circuits, there is sufficient noise to move the device output of the metastable state and into one of the two legal ones - however, this time may be large with respect to the available timing slack in the circuit resulting in a system failure. Factors that affect a flip-flop's metastable "performance" include the circuit design and the process the device is fabricated on. It turns out that by allowing sufficient settling time the MTBF for a well-designed system with asynchronous inputs can be made extremely low. This is possible since resolution time is not linear with increased circuit time and the MTBF is an exponential function of the available slack time. This can be seen in the following equation:

MTBF = e^(K2*t) / (K1 x Fclock x Fdata)
where t is the slack time available for settling, K1 and K2 are constants that are characteristic of the flip-flop, and Fclock and Fdata are the frequency of the synchronizing clock and asynchronous data. By this equation, it is clear that an increase of 't' has an exponential effect on the MTBF. The two constants account for the two key characteristics of a flip-flop's metastable behavior: the size of the window (usually sub-nanosecond and the time to get out of a metastable state that is a function of the gain-bandwidth product of the device).

EXAMPLE

Here are some calculations we did using the Chip Express CX2001 technology, based on their flip-flop parameters and example in the CX Technology Design Manual, as a look at how this technology performs. The CX2001 series uses a channeled module architecture (gate array) with each module consisting of three 2:1 muxes and an AND gate (a bit differently set up than Act 1 but not all that dissimilar). There are no hardwired flip-flops in the architecture; these are available in all Actel families except for Act 1, in Xilinx, Lucent, etc., devices. This sample calculation uses a 50 MHz clock, a 10 MHz average incoming data rate, and the available extra settling time is the independent parameter.

extra delay (nsec)	MTBF (sec)	MTBF (years)
1	448.2e-6	14.2e-12
2	180.8e-3	5.7e-9
3	72.9e+0	2.3e-6
4	29.4e+3	933.2e-6
5	11.8e+6	376.5e-3
6	4.7e+9	151.9e+0
7	1.9e+12	61.2e+3
8	779.6e+12	24.7e+6
9	314.5e+15	9.9e+9
10	126.8e+18	4.0e+12
11	51.1e+21	1.6e+15
12	20.6e+24	654.8e+15
13	8.3e+27	264.1e+18
14	3.3e+30	106.5e+21

DISCUSSION

With the 20 nSec period, let's say we allocate 10 nSec of additional delay for the first synchronizing flip-flop to recover; this leaves 10 nSec for clk->q, routing delays, t_{su}, and any unfavorable t_{skew}. Since the flip-flops in a synchronizer will be physically close, this is probably very conservative. As can be seen from the chart, 10 nSec of slack will give a pretty reliable circuit.

The information and references on this topic are available at: http://rk.gsfc.nasa.gov/richcontent/General%20Application%20Notes/mestablestates/MetastableStates.htm. Later, we'll be adding parameters for many manufacturers and a specialized calculator, for predicting MTBF for a particular design configuration.

UPCOMING TESTS

We're planning our next series of radiation tests and plan to include some new programmables. Included will be the Dyna Chip DL5000, the 0.35 µm Quick Logic pASIC 3 amorphous silicon antifuse FPGA, a standard evaluation circuit for the QYH500 series, including the digital phase lock loop (DPLL), and the UTMC amorphous silicon antifuse PAL. We also hope to include the Xilinx XC400XL devices and the Actel 42MX09. It's interesting to see the newer devices making the move to 3.3-volt systems.

RECENT TID TEST RESULTS

Below are some charts from recent total dose tests. It is noted that radiation-tolerant performance is seen in the A14100A/MEC device (5 krads(Si)/Day) and lower than typical performance is seen from the A1280A/MEC device (1 and 2 krads(Si)/Day).

IN-FLIGHT EXPERIMENT

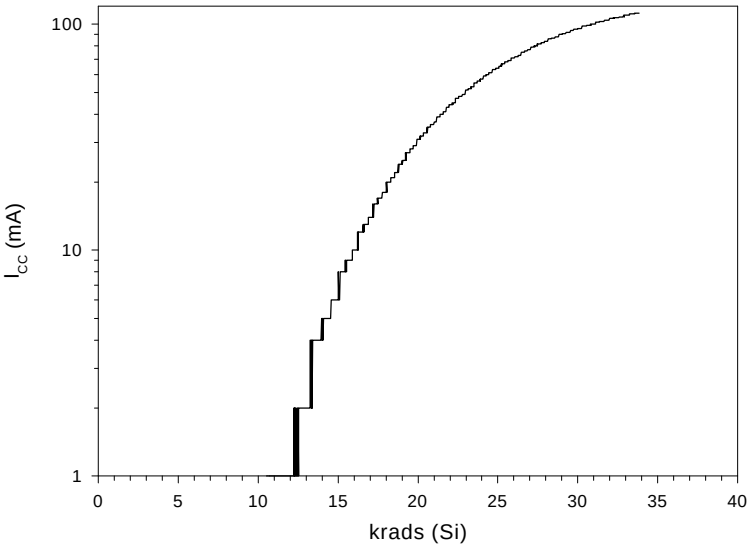
We have completed and shipped our second in a series of in-flight radiation experiments. A photograph of our flight spare unit is at the bottom of this report. This experiment includes the MKJ911 metal-to-metal antifuse FPGA technology development vehicle, the Chip Express QYH530 and the CX2041 (One-Mask) quick-turn ASICs, the amorphous silicon antifuse UTMC UT22VP10 PAL, and the Pico Systems amorphous silicon programmable substrate in an MCM with Chip Express ASICS and Harris CD4050B die.

REFERENCES AND ACKNOWLEDGEMENTS:

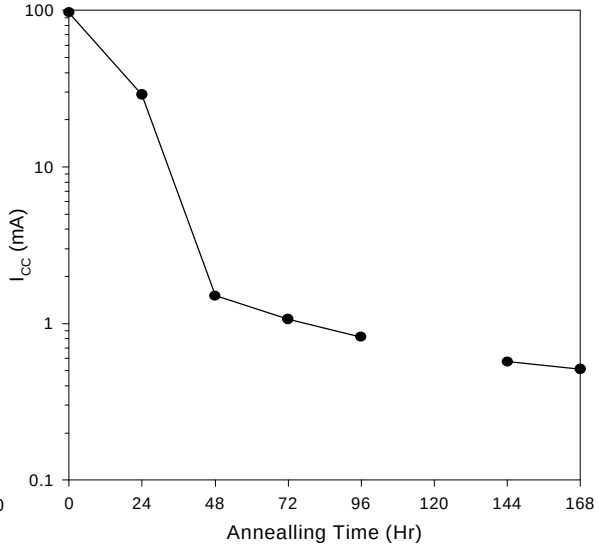
Ken LaBel - NASA/GSFC - http://flick.gsfc.nasa.gov

Anita Jeong - Actel Corp.

EO-1 A14100A/MEC TID Test
D/C 9712
UCL046
January 5, 1997
NASA/GSFC
5 krads(Si)/Day

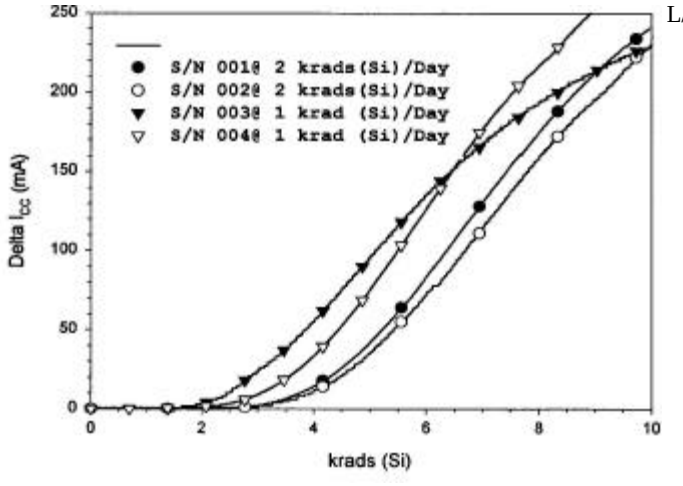


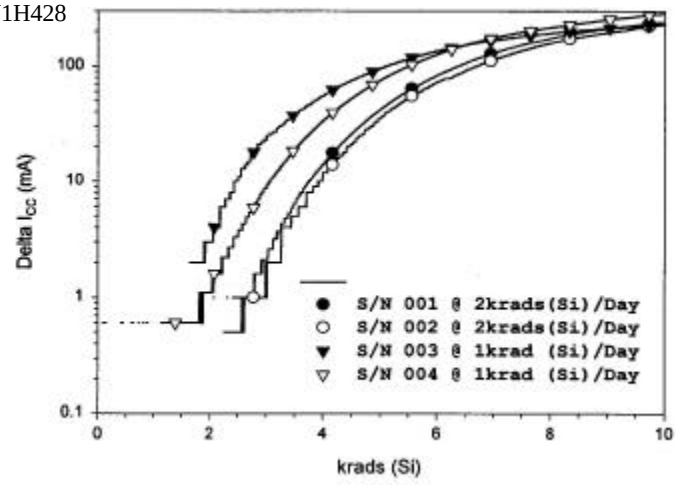
100C Annealling Data
January 12, 1998
NASA/GSFC



NOTE: The logic threshold had a slight increase of approximately 100 mV after irradiation - it decreased approximately 50 mV after the 168 hour, 100C anneal. Values ranged from 1.19V to 1.29V.

Map A1280A TID TEST
NASA / GSFC
Dec.29, 1997
2 k krads(Si) / Day for S / N 001, 002
1 krad(Si) / Day for S / N 003
D / C 9729
L/C U1H428





Note: After some unbiased annealing (facility accessibility) S/N 001 was functional and had an lcc of ~ 25mA. Under a powered, room temperature anneal, S/N 001 was tested continuously for several days and lcc dropped to ~ 18mA.

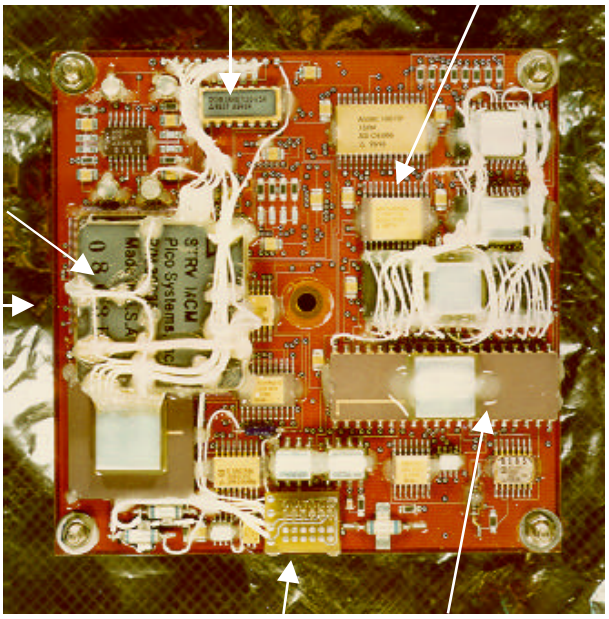
DITS-2 S/N 001 (Flight Spare)

QUAD HexFET for DUT Power Switching

UT22VP10 Amorphous Silicon Antifuse PAL

PICO SYSTEMS SUBSTRATE WITH QYH530 & CX2041 DIE

CX2041 Quick-turn ASIC under the MCM

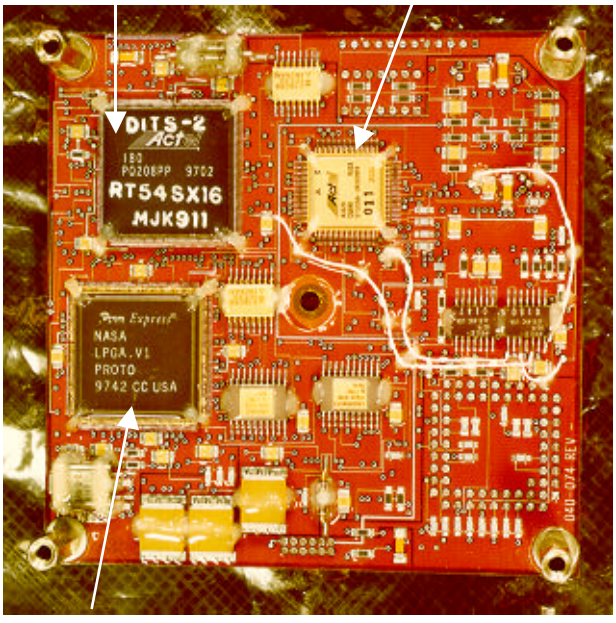


SPACECRAFT INTERFACE

80C32 uP

A1020 DUT CONTROLLER (RH1020 for S/N 002 Flight Prime Unit)

Next Generation M2M Antifuse FPGA



QYH530 Quick-turn ASIC

Jet Propulsion Laboratory
Parts Analyses

Joan Westgate
Electronic Parts Engineering Office
NASA / Jet Propulsion Laboratory
(818) 354-9529
joan.c.westgate@jpl.nasa.gov

Failure analyses (FA), destructive physical analyses (DPA) and part construction analyses (PCA) have been performed on the following part types. For a copy of the report, contact Joan Westgate (phone 818-354-9529, fax 818-393-4559 or e-mail to joan.c.westgate@jpl.nasa.gov) and request the desired document by "Log #".

FAILURE ANALYSIS

Log No.	Manufacturer	Date Code	Part Type	Part Number
6868	Linear Technology (LNT)	9152A	Operational Amplifier	RH 108AW
6877	Harris Semiconductor (HAR)	9250A	High-Speed CMOS/SOS Octal D Flip-Flop with Master Reset	54HCS273
6976	Rosemont Aerospace, Inc. (REC)	None	Temperature Transducer	ST11784-0002
6977	Solid State Devices, Inc. (SSD)	2D098	NPN Power Transistor	8838

DESTRUCTIVE PHYSICAL ANALYSIS

Log No.	Manufacturer	Date Code	Part Type	Part Number	Result
6979	United Technologies	9731	ACTS244	5962H9657101VCX	P
6980	United Technologies	9726	UTC69151	R9466304QCY	P
6982	Harris Semiconductor	9716	64K PROM, HS9-6664RH-Q	5962F9562601VYC	P
6985	International Rectifier	9729	HEXFET (S/N 48-57, 48-58, 48-59)	IRHM9130	P
6986	International Rectifier	9729	HEXFET (S/N 48-67, 48-73, 48-75)	IRHE9130	P
6987	International Rectifier	9729	HEXFET (S/N 48-97, 48-98, 48-99)	IRHE7230	P
6991	Siliconix	9718	Quad Transistor	SD50001-2	P
6995	Linear Technology	9615A	Rad Hard, Dual Precision OP-AMP	RH1013MJ8	P
7001	Harris Semiconductor	9642	Quad Receiver, 26C32	5962-F0568901VXC	P
7002	Retcon	9645	Photodiode Array	RL0128KAU	P

PART CONSTRUCTION ANALYSIS

Log No.	Manufacturer	Date Code	Part Type	Part Number
6850	Harris Semiconductor	9520	24-Bit precision Sigma Delta A/D Converter	H17190
6852	Analog Devices, Inc (ADI)	9627	3V, CMOS, 500µA Signal conditioning ADC	AD7714
6853	Burr-Brown Corporation	9621	24-Bit Delta-Sigma A/D Converter	ADS1210

Goddard Space Flight Center Parts Analyses

Listed below are the EEE parts analyses completed by the GSFC Parts Analysis Laboratory. The GSFC reports are available to NASA personnel and current NASA contractors by contacting your NASA project office.

Job Number	Manufacturer	Date Code	Part Type	Part Number	Result	Date
77293	NATIONAL SEMICONDUCTOR	N/A	LM317AT	LM317AT	P	9/25/97
78123	SEMTECH CORP	9712	SET010211	SET010211	P	4/30/97
78134	COMPENSATED DEVICES	9641	JANTXV1N5822	JANTXV1N5822	P	5/15/97
78140	BKC SEMICONDUCTORS	9704	JANTXV1N6638	JANTXV1N6638	P	5/12/97
78141	BKC SEMICONDUCTORS	9702	JANTXV1N6642	JANTXV1N6642	p	5/21/97
78151	SEMTECH CORP	9417	JANTXV1N5615	JANTXV1N5615	P	5/12/97
78235	NATIONAL SEMICONDUCTOR	9715	54LS03	M38510/30002BDA	P	8/15/97
78237	LINEAR TECHNOLOGY	9651	LT1009	JM38510/14802BXA	P	9/15/97
78240	NATIONAL SEMICONDUCTOR	9625	LM139	M38510/11201BCA	P	7/30/97
78241	OPTEK TECHNOLOGY, INC.	9644	4N45	JANTXV4N48	P	7/30/97
78245	COMPENSATED DEVICES INC.	9638	1N4122-1	JANTXV1N4122-1	P	8/14/97
78246	COMPENSATED DEIVCE INC	9625	1N4104-1	JANTXV1N4104-1	P	8/14/97
78247	HARRIS SEMICONDUCTOR	9645	HS1-248	5962R9672302QCC	P	8/29/97
78248	HARRIS SEMICONDUCTOR	9645	54LS03	5962R9672201QCC	P	8/15/97
78249	UTMC	9713	UT63M147	5962R9322603QZA	P	8/29/97
78250	UTMC	9707	UT69151E	5962R9211802QYA	P	9/10/97
78251	NATIONAL SEMICONDUCTOR	9717	54ACTQ32	5962-8973601DA	P	9/9/97
78252	NATIONAL SEMICONDUCTOR	9713	54ACTQ273	5962-8973501SA	P	9/2/97
78253	NATIONAL SEMICONDUCTOR	9634	54ACTQ04	5962-8973401DA	P	9/9/97
78254	NATIONAL SEMICONDUCTOR	9607	54ACT157	5962-8968801FA	P	8/30/97
78255	TEXAS INSTRUMENT	9710	54ALS1035	5962-8874201DA	P	9/2/97
78256	TEXAS INSTRUMENT	9710	54ALS05	5962-8854001DA	P	9/2/97
78257	NATIONAL SEMICONDUCTOR	9710	54ACT109	5962-8853401FA	P	9/10/97
78258	NATIONAL SEMICONDUCTOR	9716	54ACT244FMQB	5962-8776001MSA	P	7/30/97
78259	NATIONAL SEMICONDUCTOR	9712	54ACT240	5962-8775901MSA	P	8/30/97
78260	NATIONAL SEMICONDUCTOR	9722	54ACT00FMQB	5962-8769901MDA	P	9/9/97
78261	NATIONAL SEMICONDUCTOR	9712	54ACT245	5962-8766301BSA	P	9/30/97
78262	NATIONAL SEMICONDUCTOR	9716	54ACT374	5962-8763101SA	P	9/30/97
78263	BKC SEMICONDUCTORS	9717	1N5811	JANTXV1N5811	F	10/14/97
78264	NATIONAL SEMICONDUCTOR	9718	54ACT138	5962-8755401MFA	P	9/30/97
78265	DALE	9718	RZ090	M8340109K56R0FC	P	10/2/97
78266	DALE	9618	RZ090	M8340109K5111FC	P	10/2/97
78267	DALE	9520	RZ090	M8340109K2741FC	P	10/2/97
78268	DALE	9544	RZ090	M8340109K2211FG	P	10/2/97
78269	DALE	9649	RZ090	M8340109K1002FC	P	10/2/97
78270	DALE	9634	RZ090	M8340109K1001FC	P	10/2/97
78271	DALE	9723	RZ080	M8340108K33R2FG	P	10/2/97
78272	DALE	9529	RZ080	M8340108K2000FC	P	10/2/97
78273	DALE	9529	RZ090	M8340108L1001FC	P	9/30/97
78274	Q-TECH	9638	QT6T	M55310/16-B41A25M00000	P	9/20/97
78275	Q-TECH	9728	QT6T10	M55310/16-B41A24M00000	F	9/20/97
78277	NATIONAL SEMICONDUCTOR	9708	54AC14	M38510/75702BDA	F	8/13/97

Job Number	Manufacturer	Date Code	Part Type	Part Number	Result	Date
78279	NATIONAL SEMICONDUCTOR	9616	54ACTQ541DMQB	5962-9682901QRA	P	8/29/97
78304	SEMTECH CORP	9709	1N5811	JANTXV1N5811	P	10/14/97
78310	HARRIS SEMICONDUCTOR	9626	82C54	5962R9571301VJC	P	10/2/97
78316	HARRIS SEMICONDUCTOR	9633	CD4013	5962R9662201VXC	P	10/3/97
78317	HARRIS SEMICONDUCTOR	9624	CD4049	5962R9663601VXC	P	10/3/97
78318	HARRIS SEMICONDUCTOR	9704	HCS14	5962R9568101VXC	P	10/3/97
80535	BKC Semiconductors	9142	1N750A-1	JANTXV1N750A-1	P	10/20/97
80536	MICROSEMI	8741	1N4124	JANTXV1N4124	P	10/20/97
80603	Q-TECH	9617	HYBRID	CRYSTAL MS5310/26B32A	P	12/5/97
88000	UNITRODE	9527	UC1524AL	UC1524AL/883BC	P	12/2/97
88001	UNITRODE	9718	UC1637L/883B	5962-89957012A	P	12/2/97
88002	ANALOG DEVICES	9702, 9712, 9716	MICROCIRCUIT	AD584TH/883B	P	11/18/97
88004	NATIONAL SEMICONDUCTOR	9624A	54AC174LMQB	5962-87626012A	P	11/21/97
88005	HARRIS SEMICONDUCTOR	9723	MICROCIRCUIT	JM38510/19001BXA	P	10/8/97
88006	ANALOG DEVICES	9703	OP27AJ/883	QJM38510/13503BGA	P	10/8/97
88007	ANALOG DEVICES	9640	OP07AJ/883	QJM38510/13501BGA	P	10/8/97
88008	COMPENSATED DEVICES	9629	1N4625-1	JANTXV1N4625-1	F	9/14/97
88009	NATIONAL SEMOCONDUCTOR	9650	JL39BCA	JM38510/11210BCA	P	10/25/97
88010	TEXAS INSTRUMENT	9725	55115	JM38510/10404BEA	P	10/25/97
88011	TEXAS INSTRUMENT	9721	HCS74DMSR	JM38510/10403BEA	P	10/8/97
88012	HEWLETT PACKARD	9720	6N140A/883B	8302401EC	P	11/10/97
88014	HARRIS SEMICONDUCTOR	9544, 9640	HCS04DMSR	5962R9572501VCC	P	10/22/97
88015	HARRIS SEMICONDUCTOR	9650, 9540	HCS244DMSR	5962R9573101VRC	P	11/3/97
88016	HARRIS SEMICONDUCTOR	9606	HCS74DMSR	5962R9578201VCC	P	10/22/97
88020	HARRIS SEMICONDUCTOR	9726	HS9-1840ARH-Q	5962R9563002VYC	P	10/8/97
88021	HARRIS SEMICONDUCTOR	9714	HCS138DMSR	5962R9572701VEC	P	10/22/97
88022	HARRIS SEMICONDUCTOR	9731	HCS00DMSR	5962R9572401VCC	P	10/22/97
88023	HARRIS SEMICONDUCTOR	9703	HCS02DMSR	5962R9567901VCC	P	11/3/97
88024	HARRIS SEMICONDUCTOR	9718	HCS374DMSR	5962R9579301VRC	P	11/3/97
88025	HARRIS SEMICONDUCTOR	9709	HCS32DMSR	5962R9578101VCC	P	10/28/97
88026	HARRIS SEMICONDUCTOR	9545	HCS373DMSR	5962R9579201VRC	P	10/29/97
88027	HARRIS SEMICONDUCTOR	9605	HCS245DMSR	5962R9679701VRC	P	11/5/97
88028	HARRIS SEMICONDUCTOR	9610	HCTS139DMSR	5962R9575301VEC	P	11/4/97
88029	HARRIS SEMICONDUCTOR	9728	HCS08DMSR	5962R9568001VCC	P	11/6/97
88030	HARRIS SEMICONDUCTOR	9723	HCS164DMSR	5962R9578501VCC	P	11/4/97
88035	HARRIS SEMICONDUCTOR	9635	HCS165DMSR	5962R9578601VEC	P	11/12/97
88036	HARRIS SEMICONDUCTOR	9707	CD4024BDMSR	5962R9662803VCC	P	11/20/97
88037	HARRIS SEMICONDUCTOR	9548	HCS139DMSR	5962R9580401VEC	P	11/20/97
88038	HARRIS SEMICONDUCTOR	9650	CD4049UBDMSR	5962R9663601VEC	P	11/17/97
88039	HARRIS SEMICONDUCTOR	9642	CD4001BDMSR	5962R9582602VCC	P	12/15/97
88052	MINI-CIRCUITS	9728	HYBRID	GRA8	P	11/28/97
88057	NATIONAL SEMICONDUCTOR	9726	54ACT74FMQB	5962-8752501MDA	P	12/2/97
88058	NATIONAL SEMICONDUCTOR	9636	JM54ACT244BRA	5962/8776001BRA	P	12/2/97

Job Number	Manufacturer	Date Code	Part Type	Part Number	Result	Date
88065	SEMICON COMPONENTS, INC	9731	1N5649A	JANTXV1N5649A	P	11/14/97
88066	SEMICON INC (DC 9715) MICROSEMI CORP (DC 9730)	9715, 9730	1N5907	JANTXV1N5907	P	11/14/97
88067	MICROSEMI	9652	1N6638	JANTXV1N6638	P	12/5/97
88068	BKC SEMICONDUCTORS	9724	1N750D-1	JANTXV1N750D-1	F	12/5/97
88073	SILICONIX	9536	2N5116	JANTX2N5116	P	10/30/97
88077	MICROSEMI/WATERTOWN	9650	1N4148-1	JANTXV1N4148-1	P	10/30/97
88078	HARRIS SEMICONDUCTOR	9534	HCS21DMSR	5962R9577901VCC	P	11/6/97
88079	HARRIS SEMICONDUCTOR	9714	HCS14DMSR	5962R9568101VCC	P	11/12/97
88081	SEMTECH CORP.	9727	1N4245	JANTX1N4245	P	11/13/97
88082	ANALOG DEVICES	9712	AD390TD/883B	5962-8850902XA	P	10/31/97
88083	DALE	9736, 9718, 9704	RZ080, RZ090	M8340108K3002GG, M8340108K4701GG, M8340109K4700GG	P	12/8/97
88084	HARRIS SEMICONDUCTOR	9715	HCS08DMSR	5962R9568001VCC	P	12/15/97
88098	ANALOG DEVICES	9728	AD624SD	AD624SD/883B	P	11/25/97
88108	DALE	9716, 9627, 9636	RZ080, RZ090	M8340109K3002GC, M8340108K2201GG, M8340109K2201GC	P	12/28/97

GIDEP & NASA Advisory Impact Report

NASA Advisories, GIDEP Alerts, Problem Advisories, Safe Alerts, Product Change Notices, Diminishing Source Notices and Agency Action Notices Related to EEE Parts

GIDEP & NASA Advisory Impact Report summary will no longer be included in the EEE Links publication. For the most current information on parts issues please refer to the EPIMS database on the WWW. The URL for EPIMS-WEB is : http://epims.gsfc.nasa.gov